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Experimental Investigation of the Charge Pumping Current in Integrated MOS Transistors

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DEDICATION

To everyone

I dedicate this work

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ABSTRACT

The aim of this work is the investigation of the charge pumping technique through the variation of the gate voltage pulse width. The main part of this work is related to the investigation of the charge pumping current of MOSFETs and its dependence on the time and voltage parameters of the input gate pulses. In fact, most of the published works are based on square and / or triangular gate voltages for MOS structures or MOS transistors. The proposed technique has been applied for submicron integrated MOSFETs and many non previously published results have been obtained. Eventhough no new model has been proposed to explain the behavior of the charge pumping current on the change of the gate pulse parameters, in particular the pulse width, the model proposed by Wachnik *et al* can be slightly modified to describe the general behavior of our results. We are convinced that the results contained in this thesis can be used to improve the existing models, and consequently to explain and help in determining some of the important parameters of the Oxide-Silicon interface.

LIST OF SYMBOLS

A_G, A : gate area or channel are of a MOS transistor (cm^2).

C_D, C_d: depletion capacitance (F).

C_i : inversion capacitance (F).

c_n, c_p : the capture rates for electrons and holes respectively (s^{-1}).

C_{LF}, C_{HF} : the capacitances measured at low and high frequencies, respectively, between the gate and substrate (F).

C_{ox} : the oxide capacitance (F).

D^-, D^0 : negatively charged and neutral defect states, respectively.

$\overline{D}_{it}$: the mean surface state density averaged over the energy levels swept througn by the Fermi level ($cm^{-2}.eV^{-1}$).

$D_{it}(E_T)$: the surface state density at energy level E_T ($cm^{-2}.eV^{-1}$).

e^- : electron.

e_n, e_p : the emission rates for electrons and holes respectively (s^{-1}).

$E_{c,s}, E_{v,s}$: energy of conduction and valence band edges at surface (eV).

$E_{c,b}, E_{v,b}$: energy of conduction and valence bands in bulk (eV).

E_{finv}, E_{facc} : Fermi level positions in strong inversion and accumulation, respectively (eV).

E_F : Fermi energy (eV).

E_g : semiconductor energy band gap (eV).

E_l : the energy of the lower surface trap (eV).

E_u : the energy of the upper surface trap (eV).

$E_m(O)$: the energy of upper most-filled trap level from top of valence vand at onset of non steady state (eV).

E_T, E : trap energy (eV).

f : frequency of the applied signal (s^{-1}).

f_0 : intercept of I_{cp}/f versus $ln(f)$ plot.

f_p : a peak frequency (s^{-1}).

f_D : the universal function.

f_{T-}^- : the fractional occupancy defined as: $f_{T-}^-(E_T,t) = n_{T-}^-(t) / N_t$

$\langle G_{ii} \rangle / \omega$: the interface trap conductance averaged over band-bending variations per unit angular frequency.

I_{cp} : charge pumping current (A).

I_d : drain current (A).

K : the Boltzmann's constant (eV/K).

L : gate length (cm).

n_i : the intrinsic carrier concentration (cm^{-3}).

n_s, p_s : electron and hole concentration at the surface (cm^{-2}).

n_t^-, n_t^0 : the number of defects D^- and D^0, respectively, per unit area and are related by the relationship $D^- \leftrightarrow D^0 + e^-$. ($cm^{-2}$).

$n_{T+}^-(t), n_{T-}^-(t)$: value of n_t^- at time t during the period T_+ and T_-, respectively (cm^{-2}).

$n_{T+}^0(t), n_{T-}^0(t)$: value of n_t^0 at time t during the period T_+ and T_-, respectively (cm^{-2}).

N_A : dopant concentration in the bulk (cm^{-3}).

N_B : doping of the active regions (cm^{-3}).

N_c : effective density of states in conduction band (cm^{-3})

N_{st} : the surface trap density ($cm^{-2}.V^{-1}$).

N_t : the total number of traps per unit area ($N_t = n_t^- + n_t^0$) (cm^{-2}).

q : the magnitude of electronic charge (C).

Q_g, Q_t : the charges at the gate and in the traps, respectively per unit area (C/cm^2).

t : time (as a subscript, t indicates traps) (s).

t_f, t_r : the fall and rise times respectively of the gate signal (s).

T : the absolute temperature (K).

T_+, T_- : time period when $V_g = V_+$ and $V_g = V_-$, respectively (s).

V_D, V_d : drain voltage (V).

V_{FB} : flatband voltage (V).

V_G, V_g : gate voltage (V).

V_T : threshold voltage (V).

V_+, V_- : voltage of top edge or bottom edge of voltage pulse (V).

V_{GH}, V_{GL} : high and low level gate voltages, respectively (V).

W : gate width (cm).

w : depletion width (cm).

$\beta = q/KT$:reciprocal of thermal voltage (V^{-1}).

$\varepsilon_{ox}, \varepsilon_o$: dielectric constant of silicon dioxide.

ε_{si} : dielectric constant of silicon.

σ_n, σ : electron capture cross section (cm^2).

σ_p : hole capture cross section (cm^2).

σ_s : the standard deviation of band-bending.

ψ^+, ψ^- : the value of ψ_s during T_1 and T_2, respectively (V).

ψ_s : band-bending (or surface potential) (V).

ϕ_F : Fermi potential (V).

μ_n : the mobility of electrons ($cm^2/V\text{-}s$).

$\Delta\psi_s$: the total sweep of the surface potential during the gate pulse (V).

v_{th}, v : thermal velocity of carriers (cm/s).

α : the fraction of the period when the gate voltage is rising.

τ : pulse width (s).

Chapter 1

INTRODUCTION

Metal-Oxide-Semiconductor (MOS) transistors are the basic building blocks of MOS integrated circuits (ICs). Very Large Scale Integrated (VLSI) circuits using MOS technology have emerged as the dominant technology in the semiconductor industry. Today , Ultra Large Scale Integrated (ULSI) circuits with over 5 million transistors on a chip, with lengths of less than 0.5 microns, are in volume production [1]. As device dimensions have been reduced, models for MOS device characteristics have proved insufficient for accurate correlation to measured data, and therefore, accurate circuit simulation [1].

When designing circuits for state of the art MOS ICs, one should take into account new physical effects observed in submicrometer devices used in today's MOS VLSI technology. One knows that it is almost impossible to build a product with no defects. In present days MOS devices, with thermally grown silicon dioxide (SiO_2) on silicon (Si), some impurities or defects can be inadvertently incorporated into the oxide during oxide growth or subsequent processing steps [2-4]. This results in the oxide being contaminated with various types of charges

and traps. The most important type of charges is the interface trapped charge Q_{it} because of its wide-ranging and degrading effect on device behavior. An increase in interface trap density D_{it} causes instabilities in the MOS transistor threshold voltage and reduces the carrier mobility at the surface, which results in a reduction in the device transconductance [5].

Electrically, interface traps (also called interface states or surface states) are allowed energy states that are localized in the vicinity of the Si-SiO_2 interface, and are in electrical communication with the underlying silicon, and thus can be charged and discharged, depending on the surface potential. Although models that describe the electrical behavior of the interface traps exist, the physical origin of the traps has not been totally clarified [5,7,43]. The weight of the experimental evidence, however, supports the view that the interface traps primarily arise from unsatisfied chemical bonds at the surface of the semiconductor.

For electrical characterization of interface traps, different techniques have been developed and successfully applied in the past [8]. The aim is to be able to quantify the traps accurately so that a full understanding of the magnitude of their effects on the operational behavior of MOS devices could be achieved. Among these techniques we have high-low frequency capacitance method [2,8], conductance method [7,8], subthreshold current method [8], charge pumping technique [9-26], low-temperature capacitance method [8,27], and finally deep level transient spectroscopy technique [27]. However,

because of its applicability to small transistors, the charge pumping method uniquely lends itself to special uses. Charge pumping is one of the most reliable tools available for measuring interface trap densities in submicrometer devices found on state of the art VLSI circuits. Several variants of the charge pumping measurements principle were used for determining the average density of interface traps, their energy distribution, and their localization along the channel to describe their spatial distribution [17-24].

The present work is devoted to carry out an extensive experimentation of charge pumping measurements on submicrometer Metal-Oxide-Semiconductor Field Effect Transistors (MOSFETs) based on a variable pulse width gate voltage rather than a square- or triangular- wave gate voltage used until now. In the past, attempts to explain the effects of degradation using charge trapping only have been less successful [28-30]. More recently, it was recognized that both charge trapping and interface trap generation contribute to the degradation of device characteristics and that the influence of each mechanism is determined by the operating bias conditions. Since time constants associated with the interface traps play an important role in degradation, charge pumping experiments based on variable pulse widths have been carried out to investigate the processes of carrier capture into, and carrier release from, the interface trap.

In chapter 2, a background study of the MOS structure is presented, in which we give a brief review of the theory of the MOS transistor. This will be limited to such materials

needed for the development of models and characterization methods presented in the next chapter. As the present study involves an experimental investigation of the charge pumping current, various versions of the charge pumping technique are described in chapter 3. This technique uses the substrate current as a means to extract information about the interface states in MOSFETs. This feature, simplicity of measurements, makes this technique a best candidate for characterizing MOSFETs. In chapter 4, we describe the experimental setup used for the different charge pumping measurements. This characterization system is composed of a personal computer and different HP instruments. Testing devices on which we have carried out our experiments are integrated *n*- and *p*-channel enhancement MOSFETs with different geometries. Finally, in chapter 5, we present and discuss the different results obtained from experimentation. These results are compared with those published by other authors. Some simulation results are also presented to validate some tendencies. All these results show the charge pumping current variation with respect to different gate pulse parameters from which we can extract information about the behavior of the interface states in integrated MOSFETs.

Chapter 2

THE METAL-OXIDE-SEMICONDUCTOR STRUCTURE

2.1 Introduction

In this chapter, we present the basic theory of the Metal-Oxide-Semiconductor (MOS) structure which is the heart of the MOS technology. First, we start by studying the different charges associated with the Si-SiO_2 system especially the interface traps and their effect on the electrical characteristics of the device. Then, we calculate charges and capacitances under different regimes in the MOSFETs. Finally, we describe five of the mostly used measurement techniques to extract Si-SiO_2 interface trap density. Details of the charge pumping technique is presented in the next chapter since it is the one used in this work.

2.2 MOS Capacitor

The most useful device for the study of semiconductor interfaces is the Metal-Insulator-Semiconductor (MIS) capacitor. Another name given to this device is MOS capacitor, where 'O' stands for oxide which is thermally grown silicon dioxide (SiO_2) with a thickness that usually lies between 10 and 100nm [1,2]. Such a capacitor consists simply of a silicon semiconductor covered by an oxide layer. On the top of the oxide is a conducting layer of metal (usually aluminum) or, more commonly degenerately doped polysilicon as shown in Fig.2.1.

This basic device, which can be produced with great simplicity, can yield a great deal of information about the silicon-silicon dioxide interface.

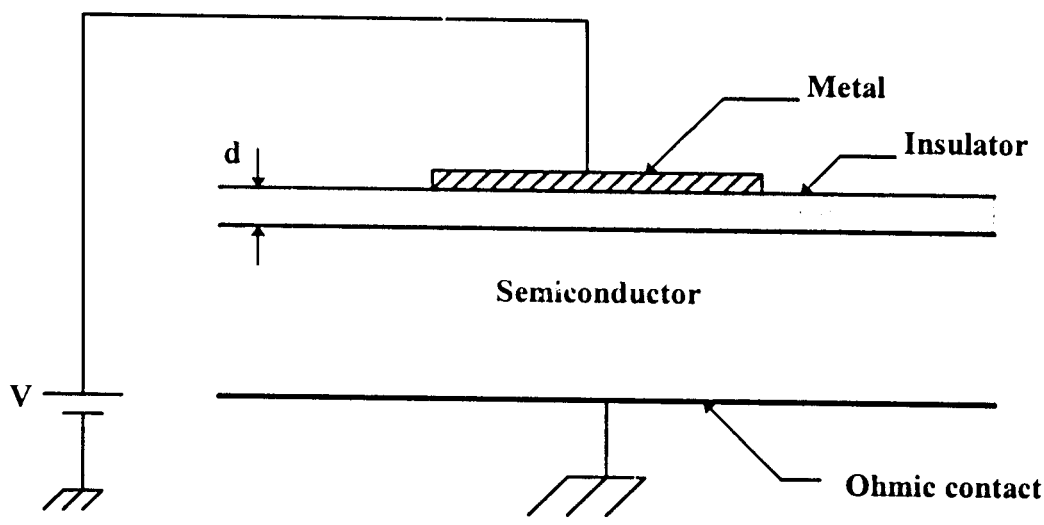

Fig.2.1 Cross section of a MIS structure
V is the applied voltage and *d* the insulator thickness

2.2.1 Oxide Charges

Some impurities or defects can be unintentionally incorporated into the oxide during oxide growth or subsequent processing steps. This results in the oxide being contaminated with various types of charges and traps [3,4]. Four different types of charges have been identified [31] in thermally grown oxide on a silicon surface. These charges are shown schematically in Fig.2.2. They are

Fixed Oxide Charges (Q_f) ,
Mobile Ionic Charges (Q_m) ,
Interface Trapped Charges (Q_{it}), and
Oxide Trapped Charges (Q_{ot}).

All these four types of charges are very much dependent on the device fabrication process.

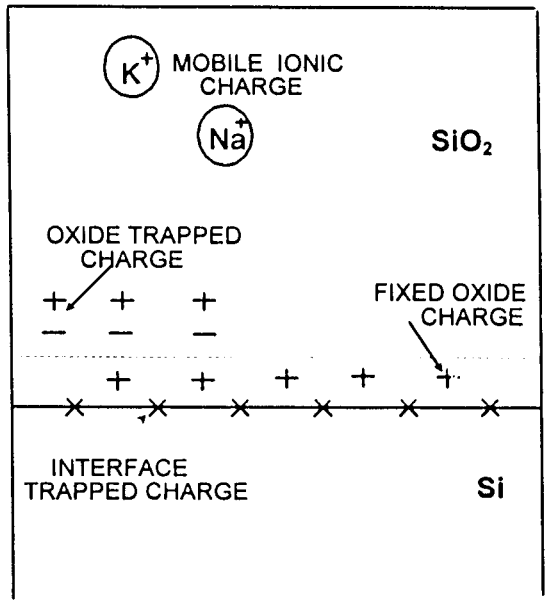

Fig.2.2 Names and locations of charges in thermally oxidized silicon

2.2.1.1 Interface Trapped Charges

It is one of the four significant charge components influencing the electrical properties of the Si-SiO_2 system. In general, the interface trapped charge is due to [31-33]

i) structural, oxidation-induced defects,

ii) metal impurities, or

iii) other defects caused by radiation or similar bond-breaking processes (e.g hot carrier effects).

However, the physical origin of the traps has not been totally clarified [1,6]. Such defects introduce unwanted energy levels in the silicon band gap which can significantly degrade the performance of MOS devices by exchanging charge with the silicon.

These types of charges have also been referred to as surface states, or interface states. Among the properties of the interface states we have [2]

i) Interface state density and its energy variation from the valence to the conduction band of the semiconductor,

ii) Capture cross sections, and

iii) Type of states (*i.e*, whether donor or acceptor).

Because interface trap levels are distributed across the silicon energy band, the interface trap density is defined as [31]

$$D_{it} = \frac{1}{q}\frac{dQ_{it}}{dE} \quad \text{number of charges/cm}^2\ \text{eV} \qquad (2.1)$$

The value of D_{it} at mid gap for silicon based modern MOS VLSI process can be as low as $5*10^9$ cm^{-2} eV^{-1} [1]. An increase in D_{it} causes instabilities in the MOS transistor threshold voltage and reduces the carrier mobility at the surface, which results in a reduction in the device transconductance [5]. The

electrical effects of interface states can be qualitatively explained as [1,34]

1) Capacitance effect : An interface state constitutes an additional allowed state at the interface. It therefore adds a capacitance of one elementary charge per state.

2) Conductance effect : capture and emission of carriers from interface states are not infinitely fast, but are associated with a time delay. This time delay can be expressed by an RC representation of the interface state. This time constant contributes to ohmic losses. Note that the ideal MOS structure does not show any losses. If such losses are present, they are most likely due to interface states.

3) Surface potential effect : The previously mentioned capacitance and conductance are AC effects. In addition to these effects, interface states cause a DC effect. The charge stored in interface states modifies the electric surface field. More applied voltage is needed to change the surface potential by a given amount when interface states are present than in the ideal case.

2.2.1.2 Other Charges

Fixed Oxide Charges (Q_f) are the immobile positive charges located within approximately 2.5nm of the Si-SiO_2 interface and normally arise from structural damage associated with oxidation or various impurity atoms. However, it is independent of the doping type and concentration in the silicon, and oxide thickness [1,31].

Oxide Trapped Charges (Q_{ot}) are associated with defects in SiO_2. The oxide traps are usually electrically neutral and are charged by introducing electrons and holes into the oxide through ionizing radiation such as implanted ions, X-rays, and electron beams. Q_{ot} resembles Q_f in that its magnitude is not a function of silicon surface potential and there is no capacitance associated with it [1,31].

Mobile Ionic Charges (Q_m) are due to sodium (Na^+) or other alkali ions that get into the oxide during cleaning, processing and handling of the MOS devices. These ions move very slowly within the oxide. Their transport depends strongly on the applied electric field (~ 1 MV cm^{-1}) and temperature (30°- 400° C), causing a shift of the flatband voltage or of the threshold voltage in the MOSFET, and may cause an unexpected device failure [1,31].

There is, however, one important difference between the interface trapped charges and the other charge components. The interface trapped charges are located at the $Si-SiO_2$ interface. Unlike fixed, mobile, or trapped charges, interface traps are in electrical communication with the underlying silicon, and thus can be charged and discharged, depending on the surface potential.

2.3 MOS Transistor

As the name Metal-Oxide-Semiconductor (MOS) suggests, the MOS transistor consists of a semiconductor substrate (usually silicon) on which is grown a thin layer of insulating oxide (SiO_2) of a thickness generally between 8 and 100nm [1,2]. A conducting layer (a metal or heavily doped polysilicon) called

the gate electrode is deposited on top of the oxide. Two heavily doped regions, called the source and the drain, are formed in the substrate on either side of the gate usually with depth values between 0.1 and 1.0μm [35]. The source and the drain regions overlap slightly with the gate. The source-to-drain electrodes are equivalent to two *pn* junctions back to back. This region between the source and drain junctions is called the channel region. Thus a MOS transistor is essentially a MOS structure, called the MOS capacitor, with two *pn* junctions on either side of the gate. MOSFETs may be either *n*-channel or *p*-channel depending upon the type of the carriers in the channel region. An *n*-channel MOS transistor (nMOST) has heavily doped n^+ source and drain regions with a *p*-type substrate and has electrons as the carriers in the channel region. While a *p*-channel MOS transistor (pMOST) has heavily doped p^+ source and drain regions with an *n*-type substrate and has holes as the carriers in the channel region.

2.3.1 Calculation of Charges and Capacitances

A typical case of an enhancement MOSFET with a *P*-type substrate is illustrated in Fig.2.3. The gate and drain are polarized by the voltages V_G and V_D referenced with respect to the source (or to the substrate because $V_B = 0$ *V*). Fig.2.4 shows the energy band diagram at thermodynamic equilibrium ($V_D = 0$ *V*), for three different situations [2,4],

1. Flat band condition : In this case, the gate voltage V_G is exactly equal to the Flatband voltage V_{FB} .This corresponds to null surface potertial. The energy bands are not curved.

2. Weak inversion threshold condition : The surface potential ψ_S is equal to the Fermi potential ϕ_F. The concentration of majority carriers at the surface p_s, and that of minority carriers n_s are equal to the intrinsic oncentration.

3. Strong inversion threshold condition : The concentration of minority carriers at the surface is equal to that of majority carriers in the volume. This corresponds to a surface potential equals to $2\phi_F$.

When a voltage greater than that of flat bands is applied to the gate, it appears under the gate, a space charge region depleted from carriers. The device is under a depletion regime and it does not conduct. Increasing the gate voltage, a minority carriers layer (electrons) is formed at the Si-SiO_2 interface, assuring thereby, the conduction of current. The condition $\phi_F \leq \psi_S \leq 2\phi_F$ defines the weak inversion regime. The strong inversion regime is defined as $\psi_S \geq 2\phi_F$. A channel with high density of electrons is then formed at the interface. The charge density Q_i of this channel and its conductance are modulated by the gate, which is known as field effect.

Now we try to calculate the depletion charge Q_d, and the inversion charge Q_i in both regimes weak and strong inversion. It must be mentioned that all calculations are performed for drain voltage tending to zero, which corresponds to function mode in ohmic regime [2,4].

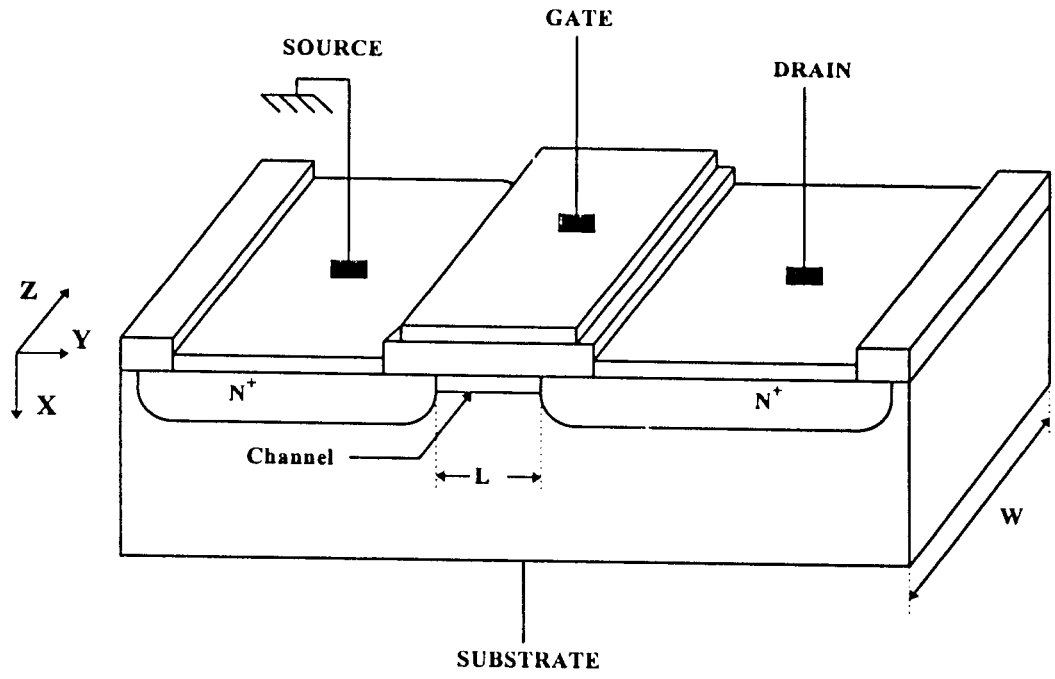

Fig.2.3 Cross section of an *n*-channel MOSFET

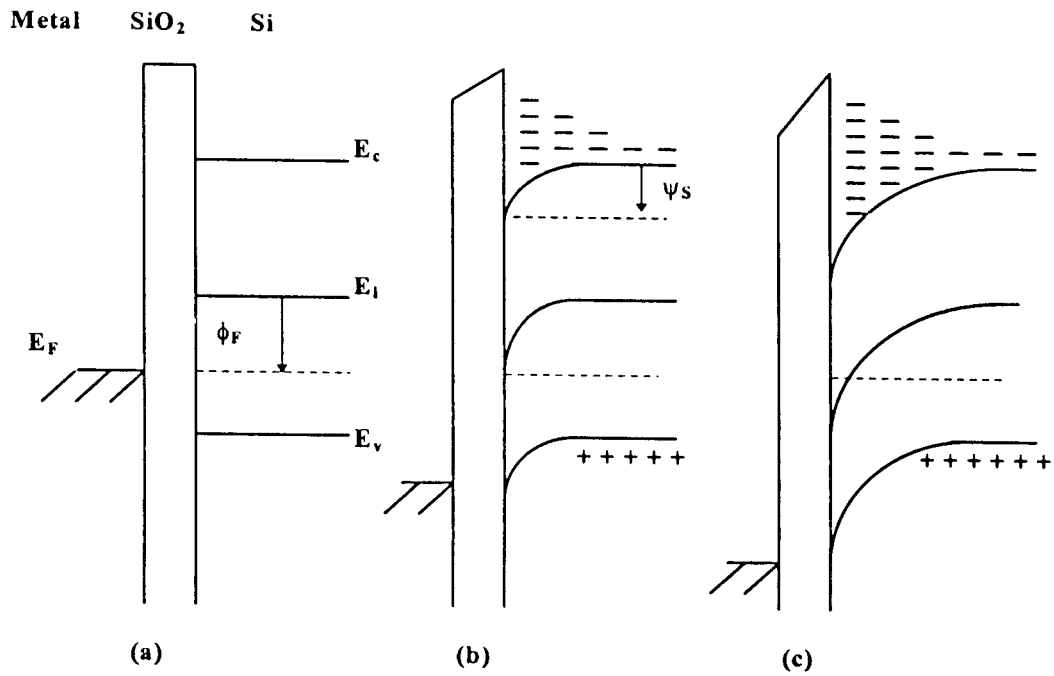

Fig.2.4 Energy band diagrams of a MOS structure
a) Flat band, b) Weak inversion, and c) Strong inversion

2.3.1.1 Depletion Regime

For potential surfaces between 0 and ϕ_F in a *P*-type substrate, the charge in the semiconductor is basically that of acceptor ions of density N_a . The electrostatic potential ψ in the substrate satisfies Poisson's equation [4]. That is,

$$\frac{d^2\psi}{dx^2} = \frac{qN_a}{\varepsilon_{si}} \qquad 0 < x < w \qquad (2.2)$$

$$\frac{d^2\psi}{dx^2} = 0 \qquad x > w \ , \qquad (2.3)$$

This form of Poisson's equation is called depletion approximation because the electron charge density is considered null. If the dopant ions are uniformly distributed in the x direction (i.e, N_a = const.), then, integrating equation (2.2) gives,

$$\psi(x) = \psi_s(1 - x/w)^2 \qquad (2.4)$$

The thickness of the depletion region w is given by [4] as,

$$w = \sqrt{\frac{\varepsilon_{si}}{\beta q N_a}(2\beta\psi_s)} \qquad (2.5)$$

The charge density in the depletion region can be expressed as [4],

$$Q_d = qN_a w \qquad (2.6)$$

The dynamic capacitance of the depletion region C_d is defined as [4],

$$C_d = \frac{dQ_d}{d\psi_s} = (1/2)\frac{Q_d}{\psi_s} \qquad (2.7)$$

2.3.1.2 Inversion Regime

In the inversion mode, Poisson's equation must be solved , taking into consideration the electrons charge which constitute the inversion layer [4]. This will give us the total charge Q_{SC} in the semiconductor after applying Gauss's law relating this charge to the perpendicular component of electric field. It could be noticed that the use of Gauss's law in this situation implies the hypothesis of null thickness of the inversion layer. A rigorous analysis has been done taking into consideration the doping inhomogeneity $N_a(x)$ and quantic considerations [36,37]. But the phenomena on which we are interested are less sensitive to these considerations. The charge density Q_i of the inversion layer are calculated with two approximations [2],

1. The inversion and depletion charges can be separated.
2. The field component E_x perpendicular to the interface is much greater than the longitudinal field component E_y .

The charge density Q_i is then the difference between the total charge Q_{SC} and the depletion charge Q_d [2,4]. So,

$$\begin{aligned} Q_i &= Q_{sc} - Q_d \\ &= \left(\frac{2\varepsilon q N_a}{\beta}\right)^{1/2} \left\{ \left[\beta\psi_s + (n_i / N_a)^{1/2} \exp(\beta\psi_s)\right]^{1/2} - \left[\beta\psi_s\right]^{1/2} \right\} \end{aligned} \qquad (2.8)$$

and the dynamic capacitance C_i associated to the inversion layer is given by [2,4],

$$C_i = \frac{dQ_i}{d\psi_s} \cong \frac{Q_i}{\eta(kT/q)} \qquad (2.9)$$

with $\eta=1$ in weak inversion and $\eta=2$ in strong inversion.

2.4 Characterization Techniques

A number of techniques have been developed to obtain surface state parameters from MOS devices. It has been noted that interface traps can significantly degrade the performance of MOS devices by exchanging charges with the silicon [1,5]. The improved understanding leads to further improvement of device performance. To understand fully the magnitude of the effect of interface traps on the operational behavior of MOS devices, it is important to be able to quantify the traps accurately.

In this section, five methods of measuring Si-SiO_2 interface trap densities are presented.

2.4.1 High-Low Frequency Capacitance Method

The high-low frequency capacitance method uses the difference in high- and low-frequency C-V characteristics measured in depletion and weak inversion to estimate a distribution of interface trap densities between flatband and threshold [2,5,8]. This technique uses the fact that the difference in measured capacitances is attributed to the inability of interface traps to respond to the small signal at high frequencies. The accuracy of this method depends on the ability to extract the interface trap capacitance from the measurements. Errors are greatest near the majority carrier band edge, where the depletion capacitance is large compared to the interface trap capacitance, and near the minority carrier band edge, where a capacitance due to the inversion layer complicates the analysis.

The interface trap density D_{it} is obtained as a function of gate bias for energies not near the band edges as [2,8]

$$D_{it} = \frac{1}{q}\left[\left(\frac{1}{C_{LF}} - \frac{1}{C_{ox}}\right)^{-1} - \left(\frac{1}{C_{HF}} - \frac{1}{C_{ox}}\right)^{-1}\right] \qquad (2.10)$$

In order to find a distribution of interface trap densities as a function of energy in the bandgap, the surface potential is used to relate the gate bias to the energies probed by the capacitance measurements.

At the expence of the tedious process of relating the gate bias to band gap energy, the high- low-frequency capacitance method is the only technique presented here which is capable of providing an interface trap distribution across the majority of the bandgap.

2.4.2 Conductance Method

The conductance method uses the interface trap conductance extracted from device capacitance and equivalent parallel conductance measurements made in depletion to estimate a distribution of interface trap densities between flatband and midgap.

The interface trap density is calculated as [7,8,27],

$$D_{it} = \left(\frac{< G_{it} >}{\omega}\right)_{f_p} \left[f_D(\sigma_s)q\right]^{-1} \qquad (2.11)$$

The process is repeated at gate biases within a range of a few kT/q of midgap and a few kT/q of flatband.
Although, it uses device admittance measurements, the conductance method is thought to be more accurate than the high- low-frequency capacitance method, since the error in the conductance method is determined by the ability to measure a single admittance and not by the difference in two admittance measurements.

2.4.3 Low Temperature Capacitance Method

The low temperature capacitance method is the newest of the techniques described in this study . It uses the difference in measured device C-V curves with and without its interface traps occupied by carriers to estimate a density of interface traps [8].

Because the rate of charge capture and emission processes for traps decreases with decreasing temperature, performing a C-V measurement at low temperature by sweeping the device from charge accumulation to deep depletion , effectively freezes the interface trap charge in place. Returning the device to thermal equilibrium , the C-V measurement is repeated with the traps full by sweeping the device back to accumulation.
A shift in voltage will result between a portion of the two measured C-V curves due to the difference in charge trapped at the interface predicted by [8,27]

$$\Delta V = \frac{q}{C_{ox}} \int_{E_v+\delta}^{E_c-\delta} D_{it}(E)dE \qquad (2.12)$$

Where δ accounts for those interface traps close enough in energy to the conduction band edge E_C and valence band edge E_V to follow the gate bias. From this, the interface trap density is calculated as [8],

$$D_{it} = \frac{\Delta V C_{ox}}{q} \tag{2.13}$$

The accuracy of this method is limited by the ability to estimate the energy range of interface traps unable to respond to the sweep of the gate bias at low temperatures.

2.4.4 Subthreshold Current Method

The subthreshold current method is the fastest, most easily performed of the methods presented. It uses the slope in the subthreshold portion of the measured drain current-gate voltage characteristic of a long channel MOSFET to estimate a mean interface trap density centered in weak inversion.
In weak inversion, drain current, as a function of gate voltage is expressed as [8]

$$I_d = \frac{W\mu_n C_{ox}^{*} n^{*}}{Lm^{*}\beta^2}\exp\left(\frac{\beta\phi_F}{2}\right)*\left[1-\exp\left(\frac{\beta V_d m^{*}}{n^{*}}\right)\right]\exp\left[\frac{\beta\left(V_g - V_g^{*}\right)}{n^{*}}\right] \tag{2.14}$$

The depletion layer capacitance can be represented as [8],

$$C_D = \sqrt{\frac{q\varepsilon_{si}\varepsilon_0 N_B}{2\left(\psi_s + \frac{kT}{q}\right)}} \tag{2.15}$$

The other parameters, n and m, are functions of the depletion layer capacitance. A superscript * signifies that the parameter is evaluated at a band-bending corresponding to midway between weak and strong inversion.

Finally, the mean interface trap density can be calculated as [8]

$$\overline{D}_{it} = \frac{1}{q}\left[\left(\frac{\frac{q}{kT}}{\frac{d\ln(I_d)}{dV_g}} - 1\right)C_{ox} - C_D^*\right] \qquad (2.16)$$

This method is limited in applicability to transistors with channel lengths greater than 20μm. The accuracy of the method is limited by the ability to estimate the doping used to calculate the device depletion capacitance.

2.4.5 Charge Pumping Method

Charge pumping technique is one of the most reliable tools available for measuring interface trap densities in submicrometer devices found on state-of-the art VLSI circuits [8]. It uses a measurable substrate current due to recombined trapped charge induced by repeatedly pulsing the gate from accumulation to inversion to characterize interface traps in MOSFETs. Because the method does not rely on admittance measurements, it is well suited for use on small transistors. A mean interface trap density representative of values between flatband and threshold is determined according to measured charge pumping current as a function of gate pulse frequency. This method has been choosen for the characterization of submicron MOSFETs in the current work. A full description of the use of this method is the subject of the next chapter.

Chapter 3

THE CHARGE PUMPING TECHNIQUE

3.1 Introduction

Due to its simplicity in the experimental level, the charge pumping technique is presented as the best candidate for characterizing the interface states in MOS transistors with small dimensions. In this technique, measurement of the dc substrate current is utilized for studying the surface states. Previous work has related the charge pumping current to the interface traps using different models. Brugler and Jespers [9] identified the source of the charge pumping current and developed a large-signal intuitive model. Backensto and Viswanathan [13] used small-signal analysis to calculate the charge pumping current. Groeseneken *et al* [14] developed a model based on the emission of carriers during the pulse transition. This model, known as transition-time technique, is the most widely used. Wachnik and Lowney [18] elaborated a model based on small rectangular voltage pulses. The proposed version of the charge pumping technique, which is the variable pulse width technique, measures the charge pumping current as a function of the frequency, amplitude, offset voltage and pulse width. So, the transition-time technique, the small

rectangular pulse technique and the variable pulse width technique give complementary information which provides a more complete picture about interface traps than either technique used alone.

However, the use of the charge pumping technique is limited only to such MOSFETs in which the ratio W/L of the width (W) and the length (L) of the gate is much larger than unity [9]. So, in this chapter, the charge pumping phenomenon is presented in some detail, where Groeseneken *et al* model [14] is presented. This model is the most widely used for the characterization of interface states. Finally, different versions of this technique are depicted.

3.2 The Charge Pumping Phenomenon

Charge pumping current has been observed for the first time in 1969 by Brugler and Jespers [9] under the form of a net direct current in the substrate during capacitance measurements carried out on *P*-channel enhancement MOS transistors. The direction of this current is opposite to that of the transistor's *p-n* junctions leakage currents. Circuit diagram for charge pumping measurements is illustrated in Fig.3.1. Source and drain are tied together and kept at a certain reverse bias voltage with respect to substrate. The gate is pulsed continuously between accumulation and strong inversion.

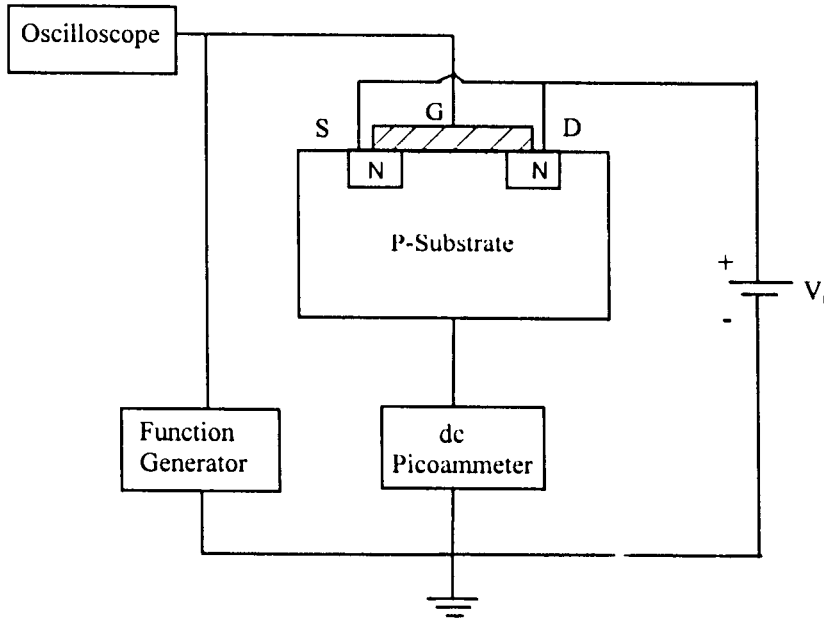

Fig.3.1 General setup for the measurement of charge pumping currents

When the gate bias increases towards strong inversion, an inversion layer will be formed due to minority carriers coming from source and drain to the channel. Some of these minority carriers (electrons in our case) are captured by the interface traps which are located below Fermi level. Going to accumulation, the minority carriers of the channel leave the surface rapidly in the direction of the two junctions under the influence of the reverse bias voltage [9,10,14].

The electrons trapped into the interface states, will recombine with the majority carriers (holes in our case) arriving from substrate. This process will induce a net current of negative charges directed from the interface toward the substrate. This current is known as the charge pumping current I_{cp} which is proportional to the number of traps at the interface.

The net charge Q_{it} pumped from the drain/source that undergoes recombination with the interface traps is given by [9] as,

$$Q_{it} = A_G q \int D_{it}(E) dE \qquad (3.1)$$

When equation (3.1) is expressed in terms of the surface potential sweep $\Delta\psi_s$, it becomes,

$$Q_{it} = A_G q^2 \overline{D_{it}} \Delta\psi_s \qquad (3.2)$$

By applying a train of pulses with frequency f to the gate, the charge Q_{it} gives rise to a current in the substrate, given by [9,10] as,

$$I_{cp} = fQ_{it} = fA_G q^2 \overline{D_{it}} \Delta\psi_s \qquad (3.3)$$

Therefore, this substrate current is caused by a recombination at the interface traps and is directly proportional to the interface trap density, the frequency of the gate pulses, and the channel area. Its magnitude increases linearly with gate pulse frequency over the limits of the measuring equipment [19]. From the measurement of this substrate current, an estimate of the mean value of the interface trap density $\overline{D_{it}}$ over the energy range swept by the gate pulse can be obtained. In order to obtain the energetic profile of interface states near the minority carriers band, Brugler and Jespers [9] have suggested to pulse the gate in strong inversion by increasing progressively the high level of the pulses whereas the low

level is kept at a constant value in accumulation. In the same way, the profile of D_{it} near the majority carriers band can be determined by fixing the high level of the pulses in strong inversion while varying the low level in accumulation. In the two cases, the energetic dependence of interface states is given by [9]

$$A_G q^2 D_{it}(\psi_s) = \frac{dQ_{it}}{dV_G}\frac{dV_G}{d\psi_s} \qquad (3.4)$$

Where $Q_{it} = \frac{I_{cp}}{f}$.

The determination of $\frac{dV_G}{d\psi_s}$ is ,then, essential to know the energetic distribution of D_{it} near the band edges of conduction and valence.

Until now, this simplified model of charge pumping does not provide too much information about other characteristics of interface states such as capture cross sections and energetic distribution of D_{it} in the middle of the forbidden band. In fact, this model is rather qualitative because, in its formulation, it does not take into account certain important phenomena such as the emission process of holes and electrons towards valence and conduction bands and also the dependence of this emision process on the charge existing at the $Si-SiO_2$ interface.

Indeed, part of the charge (electrons in our case) of the interface states does not recombine with majority carriers coming from substrate when the surface passes from strong inversion to accumulation. These electrons are emitted towards the conduction band and then collected by the source and drain

in the same way as the electrons in the channel. On the other hand, when the surface potential varies from accumulation to strong inversion, part of interface states will be charged by electrons emission from the valence band (which are furnished by the substrate) and non by electrons capture from conduction band furnished by the two junctions.

Groeseneken *et al* [14] have proposed an original model, based on transition times of pulses, for charge pumping taking into account these emission processes. Before tackling this model, one should know that the high level of the signal must be greater than the threshold voltage V_T in order to allow the device to stay in strong inversion a necessary time for charging all the interface states. In a similar manner, the low level must be less than the flatband voltage V_{FB} so that the interface states will be discharged in accumulation.

3.3 The GROESENEKEN *et al* Model

Groeseneken *et al* [14] have presented a new and accurate approach to charge pumping measurements for the determination of the $Si-SiO_2$ interface state density directly on MOS transistors. This approach is based on a careful analysis of the different processes of emission of electrons towards the conduction band and of holes towards the valence band, depending on the charge state of the interface. Furthermore, based on this insight, a new technique is developed for the determination of the energy distribution of interface states in small area transistors, without requiring the knowledge of the surface potential dependence on gate voltage.

Groeseneken *et al* [14] have considered a trapezoidal signal as illustrated in Fig.3.2. This signal has a rise time t_r , fall time t_f , period T, and an amplitude $\Delta V_G = V_{GH} - V_{GL}$, where V_{GH} being the high level of the signal and V_{GL} its low level. When $V_G = V_{GL}$, the interface states are in equilibrium with the energy bands, the surface is in accumulation and all the states located under the Fermi level are filled with electrons whereas those located above are empty.

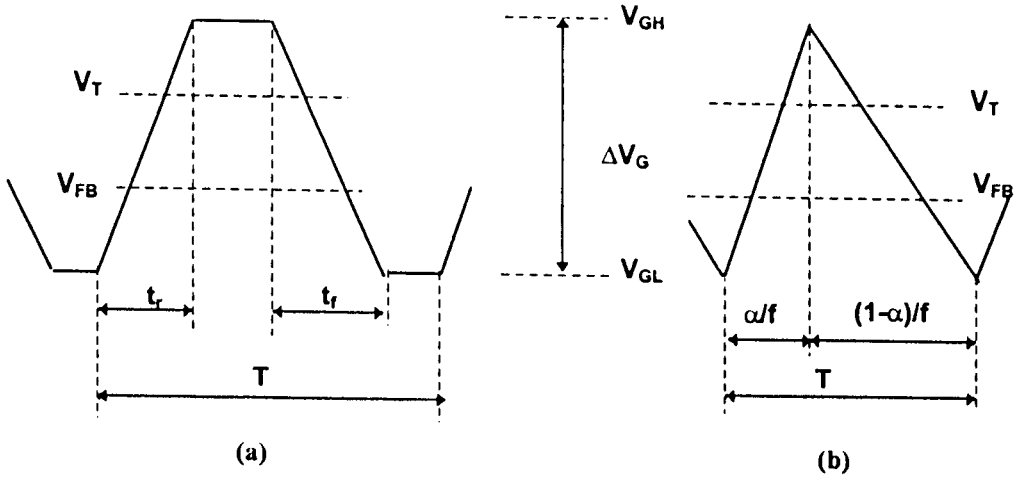

Fig.3.2 Definition of the applied gate signal parameters
(a) trapezoidal signal ; (b) triangular signal

During the rise time of the pulse, the surface potential varies with constant speed and three successive processes can be distinguished [14]:

1) At the beginning , when the Fermi level is near the valence band, the interface states will be filled by the emission of holes to this band. These holes, like those of the accumulation layer, will flow towards the substrate. This holes emission process takes place in dynamic equilibrium with the surface potential variation until the Fermi level exceeds a certain limit represented by dashed lines in Fig.3.3.

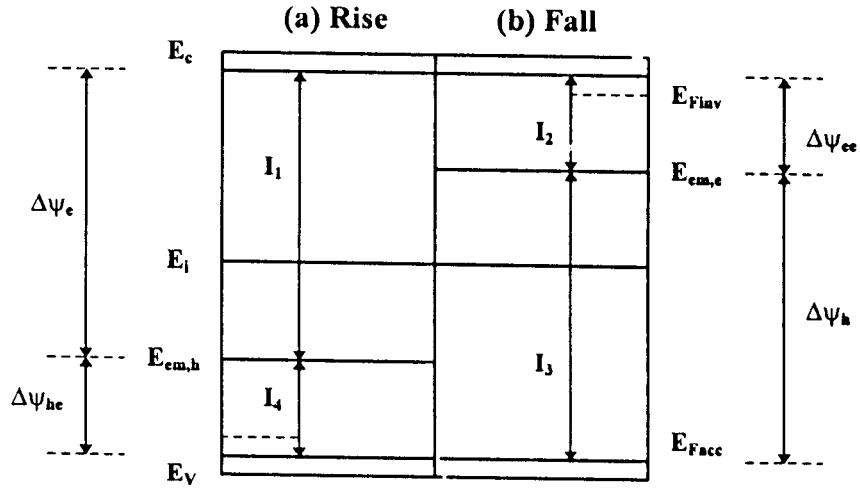

Fig.3.3 different currents flowing in the substrate during one cycle of the gate pulse

2) Beyond this limit, the interface states swept through by the Fermi level continue to be filled by the emission of holes towards the valence band, since they can not trap electrons from the conduction band. Going far from the valence band, the emission of holes towards this band can not be in dynamic equilibrium with the surface potential variation.

3) When the Fermi level at the surface exceeds the level $E_{em,h}$ the necessary time required for the interface states, located above $E_{em,h}$, to be charged by holes emission becoming very long with respect to the rise time of the signal. Hence, these states will be charged by the capture of electrons from the conduction band as soon as the Fermi level approaches the edge of this band. However, the trapping process is found to be in dynamic equilibrium with the surface potential variation just in strong inversion, when trapping time constant becomes very small. This time constant is given by [14] as,

$$\tau_n = \frac{1}{v_{th} n_s \sigma_n} \qquad (3.5a)$$

During the fall time of this signal, when the surface potential varies from strong inversion to accumulation, we can distinguish similar mecanisms. First, electrons are emitted by interface states to the conduction band and are collected by the source and drain. This emission process is first produced in dynamic equilibrium with the surface potential variation. Then, non-equilibrium electrons emission will take place until the Fermi level reaches the value $E_{em,e}$ whose position depends on t_f . Beyond this limit, the necessary time for discharging the interface states, by electrons emission, becomes very important and these states will be discharged by the capture of holes from the valence band, where the Fermi level is close enough to this band. At the beginning, this trapping process, which corresponds to a recombination electron-hole, takes place in an non-equilibrium manner, then, as soon as Flatband condition is reached, holes density becomes high enough, and equilibrium is established. The time constant of holes capture is given by a similar relationship to τ_n as [14],

$$\tau_p = \frac{1}{v_{th} p_s \sigma_p} \qquad (3.5b)$$

Hence, there exists four different currents associated to the regimes described above given by [14] as,

$$I_1 = -q^2 \overline{D}_{it} \Delta\psi_e f A_G \qquad (3.6a)$$

$$I_2 = q^2 \overline{D}_{it} \Delta\psi_{ee} f A_G \qquad (3.6b)$$

$$I_3 = -q^2 \overline{D}_{it} \Delta\psi_h f A_G \qquad (3.6c)$$

$$I_4 = q^2 \overline{D}_{it} \Delta\psi_{he} f A_G \qquad (3.6d)$$

Where, $\Delta\psi_e = E_{Finv} - E_{em,h}$,

$\Delta\psi_{he} = E_{em,h} - E_{Facc}$,

$\Delta\psi_{ee} = E_{Finv} - E_{em,e}$, and

$\Delta\psi_h = E_{em,e} - E_{Facc}$

The net current that will flow in the substrate is the sum of the current I_4 , due to the holes emission towards the valence band and which are collected by the substrate during the rise time of the signal, and the current I_3 resulted from the capture of holes furnished by the substrate during the fall time is calculated as [14]

$$I_{sub} = I_{cp} = I_4 + I_3 = q^2 \overline{D}_{it} \left(\Delta\psi_{he} - \Delta\psi_h \right) f A_G \qquad (3.7)$$

It should be noted that Groeseneken *et al*, when writing equations (3.6), have assumed a uniform distribution of interface states in the forbidden band.

In order to determine the levels $E_{em,e}$ and $E_{em,h}$, Groeseneken *et al* have utilized the classical theory of carriers emission,

$$E_{em,e} - E_i = -kT \ln\left[v_{th} \sigma_n n_i t_{em,e} + \exp\left(\frac{E_i - E_{Finv}}{kT} \right) \right] \qquad (3.8a)$$

$$E_{em,h} - E_i = kT \ln\left[v_{th} \sigma_p n_i t_{em,h} + \exp\left(\frac{E_{Facc} - E_i}{kT} \right) \right] \qquad (3.8b)$$

where $t_{em,e}$ and $t_{em,h}$ are the non-equilibrium emission times for electrons and holes respectively. These emission times were approximated by [14] as,

$$t_{em,e} \cong \frac{|V_{FB} - V_T|}{|\Delta V_G|} t_f \qquad (3.9a)$$

$$t_{em,h} \cong \frac{|V_{FB} - V_T|}{|\Delta V_G|} t_r \qquad (3.9b)$$

These two equations are based on the following approximation : the critical level, represented by dashed lines in Fig.3.3a , beyond which emission of holes becomes out of dynamic equilibrium, is very close to the Fermi level in Flatband conditions. In the same way, the critical level for electrons emission in dynamic equilibrium, represented by dashed lines in Fig.3.3b, is approximated by the Fermi level in the threshold of the strong inversion.

For triangular signals, expressions become as, [14]

$$t_{em,e} \cong \frac{|V_{FB} - V_T|}{|\Delta V_G|} \frac{1}{f} \alpha \qquad (3.10a)$$

$$t_{em,h} \cong \frac{|V_{FB} - V_T|}{|\Delta V_G|} \frac{1}{f} (1-\alpha) \qquad (3.10b)$$

The charge-pumping current I_{cp} comes out in the case of square pulses for *n*-channel transistors (rise and fall time are not neglected) as, [14]

$$I_{cp} = 2q\overline{D_{it}}fA_G kT\left[\ln(v_{th}n_i\sqrt{\sigma_n\sigma_p}) + \ln\left(\frac{|V_{FB}-V_T|}{|\Delta V_G|}\sqrt{t_f\, t_r}\right)\right] \qquad (3.11a)$$

and for sawtooth pulses as, [14]

$$I_{cp} = 2q\overline{D_{it}}fA_G kT\left[\ln(v_{th}n_i\sqrt{\sigma_n\sigma_p}) + \ln\left(\frac{|V_{FB}-V_T|}{|\Delta V_G|}\frac{1}{f}\sqrt{\alpha(1-\alpha)}\right)\right] \qquad (3.11b)$$

The same formulas apply for a *p*-channel transistor, just by inverting the sign of the charge-pumping current. These formulas are valid for charge-pumping measurements in normal conditions, *i.e*, without taking into account special effects such as the decreasing current with frequency for very high frequencies (above a few megahertz) [14].

The total recombined charge of the interface states per unit cycle Q_{it} that gives rise to the charge pumping current is expressed as

$$Q_{it} = \frac{I_{cp}}{f} \qquad (3.12)$$

On a semilogarithmic plot, its dependence on frequency is just a straight line when applying triangular pulses to the gate. This gives, from equation (3.11b),

$$Q_{it} = 2q\overline{D_{it}}A_G kT\left[\ln(v_{th}n_i\sqrt{\sigma_n\sigma_p}) + \ln\left(\frac{|V_{FB}-V_T|}{|\Delta V_G|}\frac{1}{f}\sqrt{\alpha(1-\alpha)}\right)\right] \qquad (3.13)$$

From the extrapolation of this curve to zero charge, the obtained frequency f_0 gives a value for the geometrical mean value of the capture cross sections.
Thus, for $Q_{it} = 0$ in (3.13), we obtain,

$$\sqrt{\sigma_p \sigma_n} = \frac{1}{v_{th} n_i} \frac{|\Delta V_G|}{|V_{FB} - V_T|} \frac{f_0}{\sqrt{\alpha(1-\alpha)}} \qquad (3.14)$$

In another way, the energetic profile of interface states can be obtained by varying the rise and fall times of the trapezoidal signal. The slope of the curve can be expressed as [14]

$$\frac{dQ_{it}}{d\log f} = \frac{2qkT\overline{D_{it}}}{\log e} A_G \qquad (3.15)$$

This allows the determination of the mean value of the surface state density $\overline{D_{it}}$ using just the values of temperature and the gate area of the transistor. However, the determination of the energetic profile of interface states by the variation of t_r and t_f are not valid in all the forbidden gap, since σ_n and σ_p are supposed to be independent of energy, this is valid only in midgap. Groeseneken *et al* used the same values for σ_n and σ_p because their model can estimate only the geometric mean value $\sigma = (\sigma_n \sigma_p)^{0.5}$. This approximation could be serious since σ_n can reach values of hundreds times that of σ_p [41].

3.4 The Wachnik *et al* model

This charge pumping current, which is due to small rectangular pulses and whose model is based on Shockley-Read-Hall traps, can be used to determine the density, the electron capture cross section, and the hole capture cross section of interface traps near midgap [18].

Consider the gate signal shown in Fig.3.4. Let the transition from one level to the other be fast enough so that traps neither emit nor capture during the transition and assume that the surface is pulsed about midgap. During the period T_+ , which corresponds to gate voltage V_+ , the surface is weakly inverted and traps capture electrons from the conduction band and emit holes to the valence band. In the same way, during the period T_- , after the inversion layer disappears, holes are captured from the valence band by the electron-filled traps and electrons are emitted by traps to the conduction band.

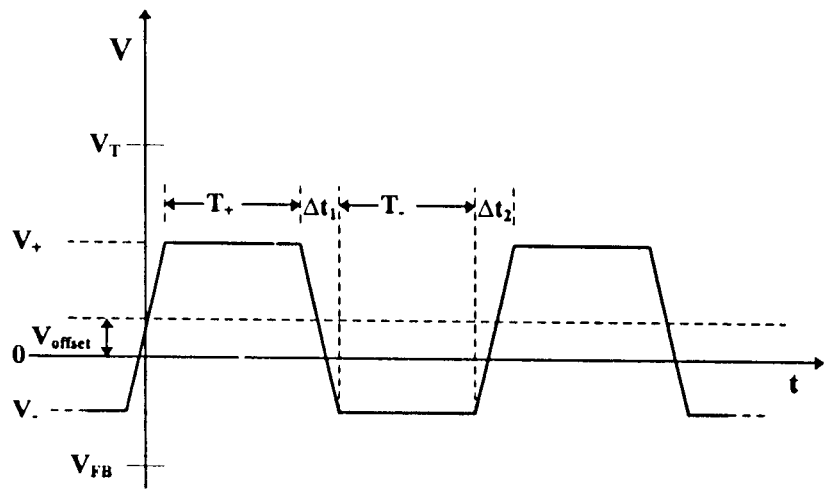

Fig.3.4 Small rectangular signals applied to the gate during charge pumping

The processes by which the carriers in the bulk fill and empty the traps determine the charge pumping current as it is illustrated in Fig.3.5 and Fig.3.6. Capture of a carrier from one band followed by emission of the carrier to the same band does not contribute to the net flow of current. Emission of a carrier followed by emission of an opposite sign carrier gives rise to the thermally generated leakage current. This leakage current flows from the substrate through the external circuit to the source and drain. A recombination process consisting of capture of a carrier from one band followed by capture of a carrier from the other band gives rise to a net current flow with direction opposite to the thermally generated leakage current. This current due to recombination is the charge pumping current. The model of the charge pumping current due to small rectangular pulses is presented in chapter 5.

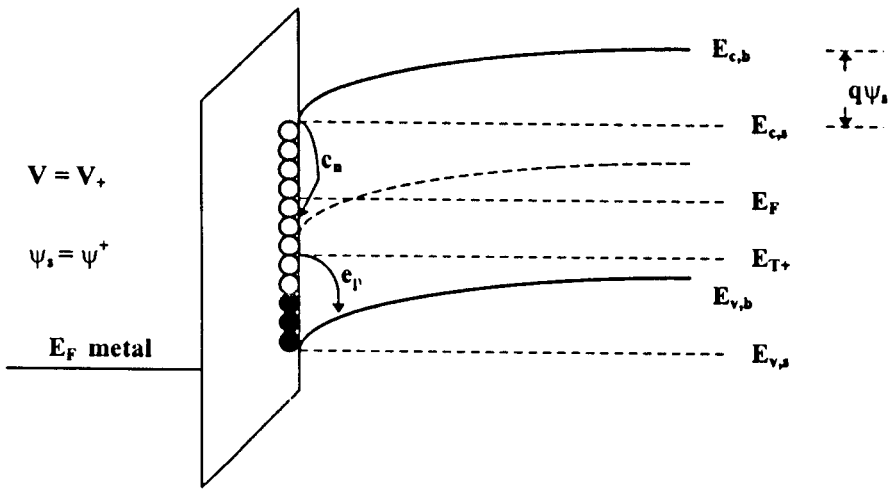

Fig.3.5 Electron capture and hole emission .

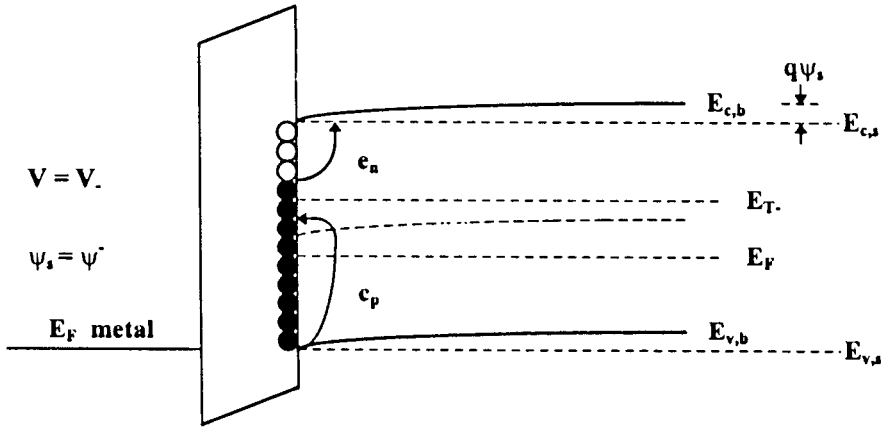

Fig.3.6 Hole capture and electron emission .

3.5 Other Versions

The commonly used version of the charge pumping method was introduced by Elliot [11]. It consists of applying a constant reverse bias voltage at source and drain, while sweeping the base level of the gate pulse train from a low accumulation level to a high inversion level. The amplitude, the frequency, and the rise and fall times of the pulses are kept constant. As a result five operating regions can be distinguished in the behavior of the substrate current as a function of the base level of the gate pulses [19].

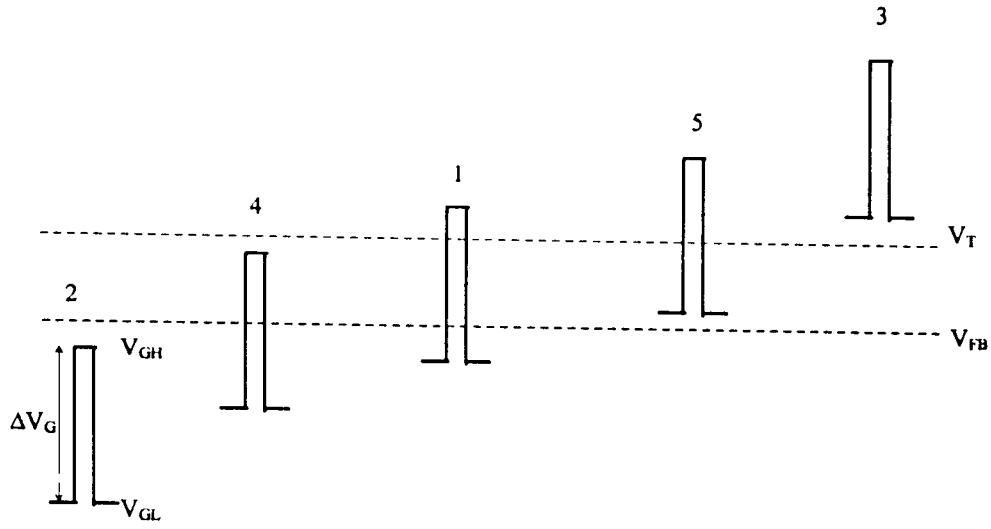

Fig3.7 Illustration of the measurement method for the case of an n-channel MOSFET

In region 1 ($I_{cp} = I_{cp,max}$) , the base level V_{GL} is lower than the flatband voltage V_{FB} while the top level of the pulse V_{GH} is higher than the threshold voltage V_T , the conventional charge pumping effect occurs. This means that a net amount of charge is transferred or pumped from the source and the drain to the substrate via the fast interface traps each time the transistor is pulsed from inversion toward accumulation and back. However, in region 2, the top and base levels of the gate pulse train are below the flatband voltage. Therefore, the fast interface traps are permanently filled with holes, and consequently no recombination current is measured. In region 3, the channel is permanently in inversion, so no holes reach the surface at any time. For both cases, the measured substrate current consists of only the source and drain leakage currents. For region 4, the charge pumping current increases from zero to a saturation level. From the principle of the charge pumping effect, it can

be easily understood that the recombination process disappears when going from region 1 to region 2 because the electron concentration at the interface during the inversion part of the gate pulse drastically reduces when the top level does not reach V_T .

Charge-pumping measurements have been performed in different ways :

Method 1 by keeping the pulse base level in accumulation and pulsing the surface into inversion with increasing amplitudes [9].

Method 2 by varying the pulse base level from inversion to accumulation while keeping the amplitude of the pulse constant [11].

Method 3 by keeping the pulse base level in inversion and pulsing the surface into accumulation with increasing amplitude [38].

Chapter 4

EXPERIMENTAL SETUP

4.1 Introduction

In this chapter we will first describe the different elements of the device characterization system that has been used in the different charge pumping measurements. This system consits of a personal computer linked to the different HP instruments through the IEEE 488 interface bus. All manual settings on the HP instruments can be programmed by the personal computer which acts as a system controller. Then, we present the experimental setup for measuring the device data that are required. Finally, we discuss the different experimental results primarily obtained for the system calibration.

4.2 Device Characterization System

Measurements are performed using the general setup shown in Fig.4.1 below, [42]

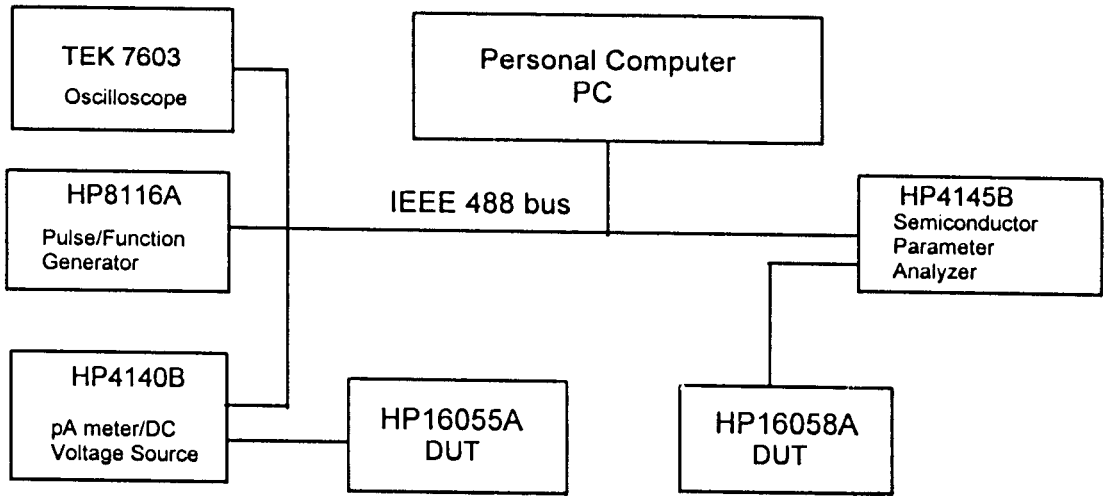

Fig.4.1 Setup for different charge pumping experiments

This characterization system consists of :

4.2.1 The HP 4145B Semiconductor Parameter Analyzer

It is a fully automatic, high performance, programmable test instrument designed to measure, analyze, and graphically display the dc characteristics of a wide range of semiconductor devices, such as diodes, bipolar transistors, field effect transistors, wafers, and integrated circuits. Its main applications include computer aided design of integrated circuits, new device evaluation, materials evaluation, component selection for circuit design and quality control.

It is equipped with four programmable source/monitor units (SMU), two programmable voltage source units (Vs), two voltage monitor units (Vm), a fully interactive graphics display, removable flexible disc storage, softkeys, full arithmetic keyboard, and an HP-IB interface bus.
Each SMU channel has three modes of operation : voltage source/current monitor (V), current source/voltage monitor (I), and common (COM). Source voltage and source current can be held constant or swept linearly or logarithmically. When used as a voltage source/current monitor (V mode), each SMU can be programmed to output DC voltages from 0V to ± 100V over three ranges, with a resolution of 1mV max. When used as a current source/voltage monitor (I mode), each SMU can be programmed to output currents from ± 1 pA to ± 100mA over nine ranges, with a resolution of 1pA max.

Furnished with the HP 4145B Semiconductor Parameter Analyzer, is the HP 16058A test fixture, a specially designed shielded box which connects to the HP 4145B's rear pannel. The HP 16058A is equipped with a light shielded lid to allow stable measurement of light sensitive devices and to prevent electromagnetic interference with the device under test (DUT). This measuring unit is used to have the full characteristics of transistors and to test the quality of the gate oxide before any charge pumping measurement. It can be used on the bench or as part of a complete measurement system in the laboratory.

4.2.2 The HP 4140B pA Meter/DC Voltage Source

This measuring equipment comprises a high stability pAmeter with 10^{-15} A maximum resolution coupled with two programmable dc voltage sources. It allows stable and fast (less than 35 ms at 1nA) measurements thanks to the use of a variable digital integration method which is very usefull for the measurement of the small leakage currents of semiconductor devices and the static characteristics of field effect transistors.

One of the two programmable dc voltage sources (V_A) can operate not only as a programmable dc voltage source but also as a unique staircase and accurate ramp generator.

The HP 4140B provides analog output which can be used to output analog data to an x-y recorder and to trace I-V/C-V curves. The HP 4140B also provides HP-IB interface. This instrument is connected to the HP 16055A test fixture via three test leads or channels. For low level of current measurements in the pA range, a triaxial cable must be used. It is a double shielded coaxial in which the center conductor is surrounded by two concentric, independent shield conductors. It helps in maximizing the attenuation of radiated signals and minimizes the pickup of external interference.

4.2.3 The HP 8116A Pulse/ Function generator

This sophisticated equipment is used to generate the desired signal with an appropriate amplitude, frequency, duty cycle (pulse width) and dc offset. It can generate sinewave signals, sawtooth (triangular) signals, square signals, as well as pulses with different widths.

The HP 8116A can supply a high frequency signal of a maximum frequency equal to 50 Megahertz.

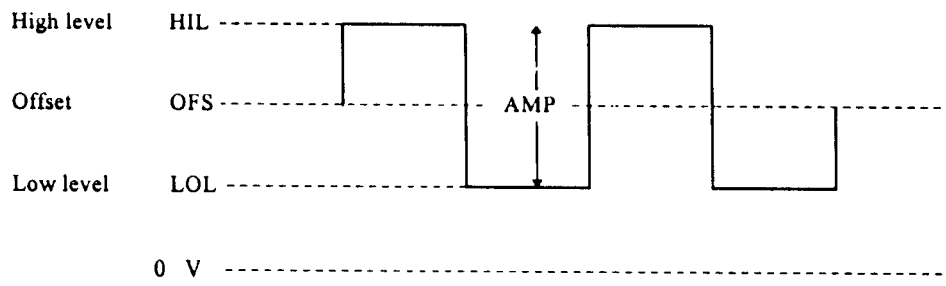

Fig.4.2 Level parameters of a gate pulse

4.2.4 The TEK. 7603 Oscilloscope

This oscilloscope is designed for general purpose measuring applications. It has three plug in compartments that accept different plug in units to form a complete measurement system. The flexibility of this plug in feature and the variety of plug in units available allow this system to be used for many measurement applications. It has an input impedance of 10MΩ, 20pF ,a deflection factor of 5mV to 5V/div, and a sensitivity of 1mV and 0.1 μsec. This instrument is used, in our case, to display the shape of the signal and eventually to check its amplitude and period.

4.2.5 The Test Fixture Boxes(HP 16055A and HP 16058A)

These test-fixture boxes with their corresponding accessories and cables are used. However, the test-fixture boxes allow only the use of encapsulated devices. Devices under test (DUT) are protected against electromagnetic and light noises when they are mounted within these boxes.

4.2.6 The IEEE-488 Bus

The elements of the characterization system are linked together with an IEEE-488 bus. It is an international standard governing byte serial bit parallel interface systems for instruments. It is also known as the general purpose interface bus, GPIB, the Hewlett Packard interface bus, HPIB, IEEE Bus, and even the ASCII Bus.

The IEEE-488 bus is used to interconnect up to 15 instruments. Each device on the bus is connected to 16 signal lines and 8 ground lines on the bus. These 16 signal lines can be considered as three separate groups. Eight of the lines are used to carry data and commands. Three lines control the transfer of the data. Whilst the remaining five lines are for general interface management.
So, the IEEE standard 488 specifies a digital interface for programmable instrumentation, ie, it is a way of interconnecting electronic measuring and control apparatus.

4.2.7 The PC Elite IEEE-488 Interface Card

This card is used as an interface through which the host computer is linked to the IEEE-488 bus, and hence to all the elements of the characterization system. PC Elite IEEE-488 gives the PC user precise control over a huge range of industry standard IEEE-488 devices. It is a half size card that fits any PC or AT slot. PC Elite card has the complete controller, Listener, and talker ability.

The companion product for the Elite card is the Professional-488 (Pro-488) Device Driver development environment. The Pro-488 software system allows any PC with an IEEE-488 interface to become an IEEE bus controller, exercising complete control over a bus full of up to 14 IEEE instruments. This makes the Pro-488 a good development environment for IEEE besed data aquisition and control. Finally, PC Elite is fully compatible with many software applications (Lab Windows, DaDisp) and langages (Pascal, C, Assembler) that run under Windows or DOS.

4.2.8 The Personal Computer

It acts as a system controller of the overall settings over the whole range of the compatible equipments and instruments. The PC is used first to set the different instruments with an appropriate setup , then to read the data obtained from the different measurements, and finally store the data in an appropriate files for an eventual analysis. Various programs have been already developed using the Pascal langage (not in this work) to achieve the above mentioned tasks.

4.2.9 Testing devices

The devices on which we have performed our measurements consist of a number of *n*- and *p*-channel MOSFETs having the following characteristics

Channel lengths	L= 0.4 to 0.8 μm
Channel width	W= 4 μm.
Oxide thickness	12 nm
Gate	Polysilicon
Technology type	0.5 μm

4.3 Experimental Measurements

The general setup we have built to perform our experiments is shown in Fig.4.1. The generator we have used is the HP 8116A Pulse/Function generator of maximum frequency 50Mhz to generate the needed waveforms with the desired frequency, duty cycle, pulse width, dc offset, and amplitude. The shape of the signal and its position are displayed on the Tek.7603 oscilloscope. The HP4140B pA/DC Voltage Source is used to measure the charge-pumping current as well as to supply a variable output voltage through its both programmable sources V_A and V_B. Also used in these experiments, is the HP4145B Semiconductor Parameter Analyser to have the full characteristics of transistors and to test the quality of the gate oxide before any charge pumping measurement.

The charge pumping measurements have been performed in different manners, depending on the gate voltage signal applied to the MOS transistor as shown in Fig.4.3. The choice

of the waveform parameters such as frequency, duty cycle, pulse width, amplitude, offset, and the biasing voltage V_r is of great importance. Thus, a large set of experimental data has been obtained for charge pumping current for different parameters of the gate signal.

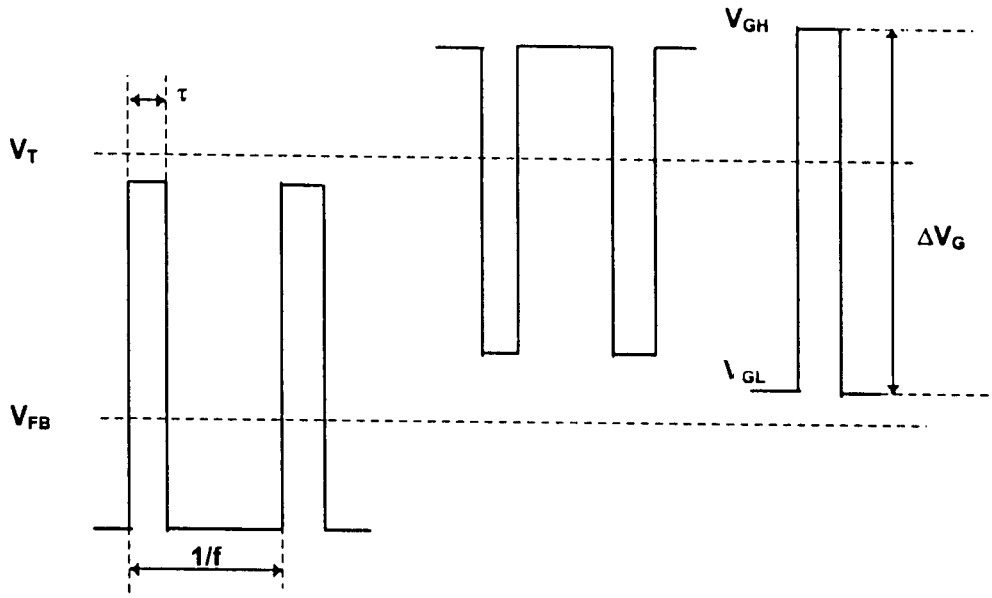

Fig.4.3 Illustration of the voltage signal applied to the gate

4.4 System Calibration

before starting charge pumping measurements, we make sure that our characterization system works well or needs some calibration. For this reason, many active and passive devices have been characterized, some of the measured electrical characteristics are shown in Fig.4.4, Fig.4.5, and Fig.4.6, for a resistor, a zener diode, and a bipolar transistor.

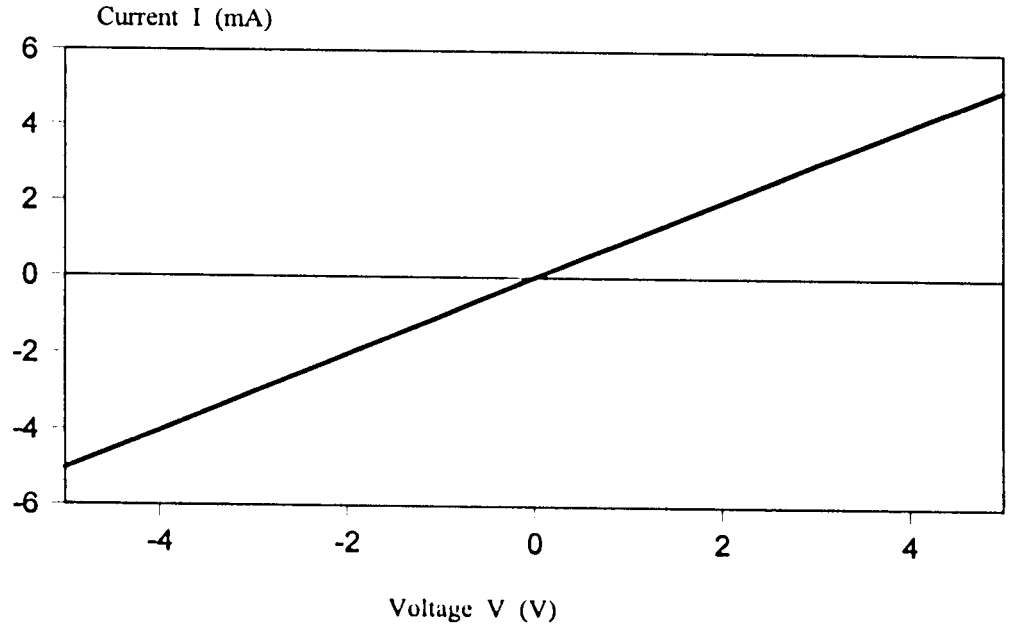

Fig.4.4 I-V characteristic of a 1 KΩ resistor

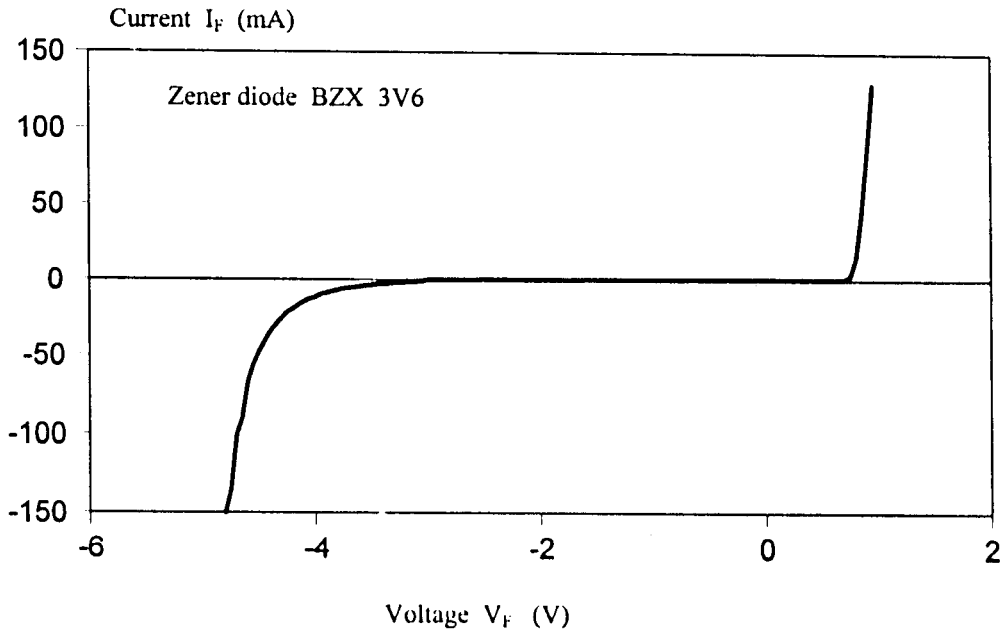

Fig. 4.5 I-V characteristic of a Zener diode

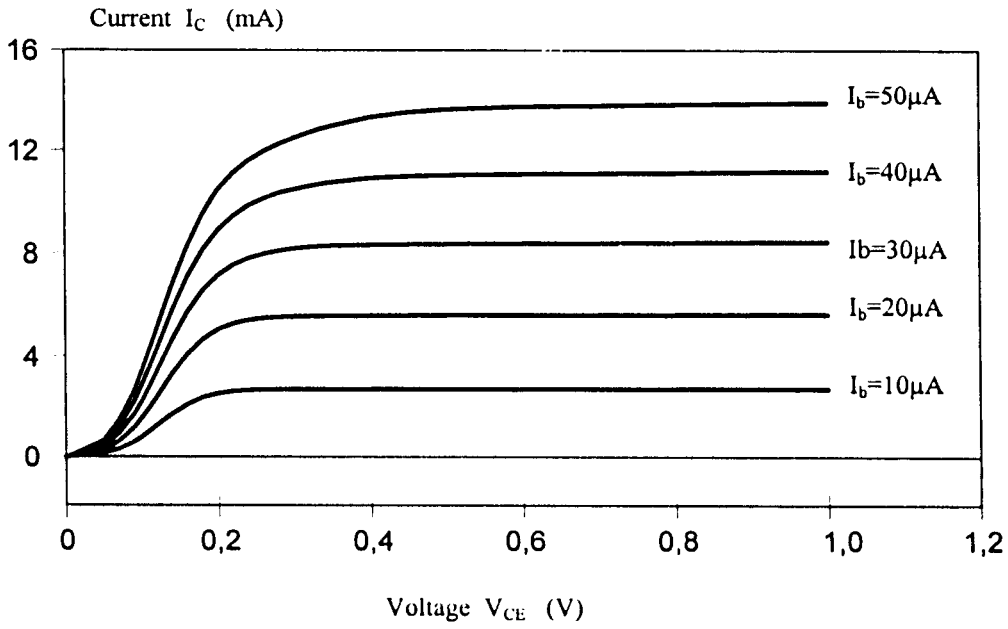

Fig.4.6 Transfer characteristics of a bipolar transistor (BC 548)

Chapter 5

RESULTS AND DISCUSSION

5.1 Introduction

The setup described in the previous chapter has been used to carry out all the experiments we have performed on our devices.

We have started firstly to reproduce some of the results that have been reported by previous authors. And secondly, we have tried to perform the measurements by changing each time the value of the gate pulse width for different frequencies and various pulse voltage levels. The devices on which we have carried out our experiments are integrated transistors of channel lengths between 0.4 to 0.8μm, channel width 4μm, oxide thickness of 12nm, polysilicon gate material, and fabricated using the 0.5μm technology.

5.2 Elliot's Curves

The first step we have performed was to get the curves shown in Fig.5.1 known as The Elliot's curves. They show the change of the charge pumping current I_{cp} versus the lower value of the gate voltage for different pulse amplitudes and a given frequency. The gate pulses we have used are square pulses with a frequency of 20Khz and a reverse source-drain voltage of 0.1V. The duty cycle δ for the input signal is selected to be 50%.

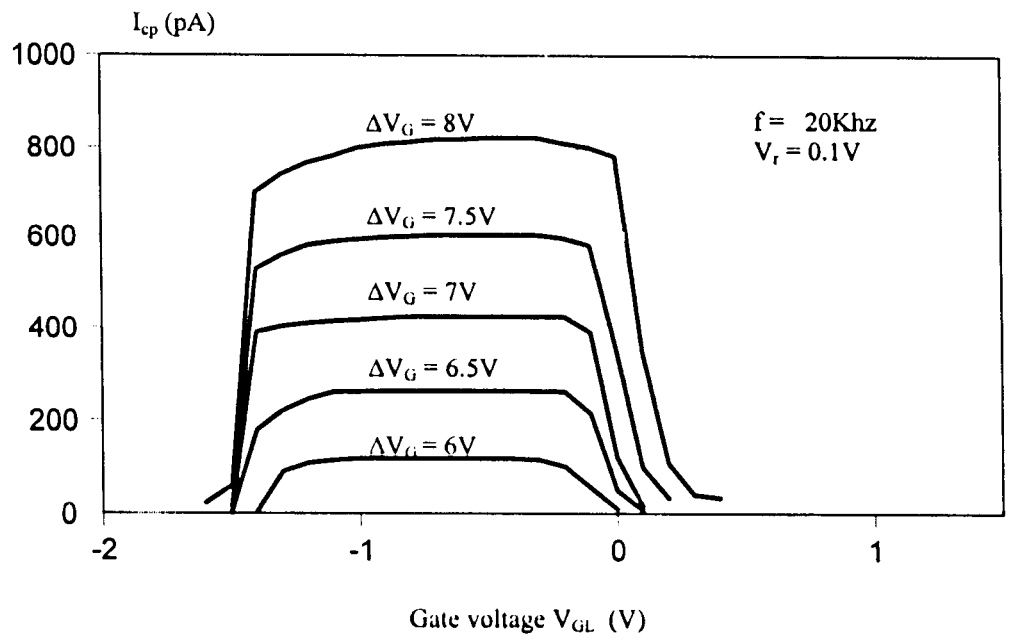

Fig.5.1 Charge pumping current I_{cp} versus lower gate voltage V_{GL}, for $f = 20Khz$, $V_r = 0.1V$,

The other curves which are shown in Fig.5.2 show the Elliot's curves for different values of V_r and a fixed pulse amplitude ΔV_G =5V. The frequency of operation for these curves is fixed to 10Khz and the pulse's lower level changes from 0V to -6V.

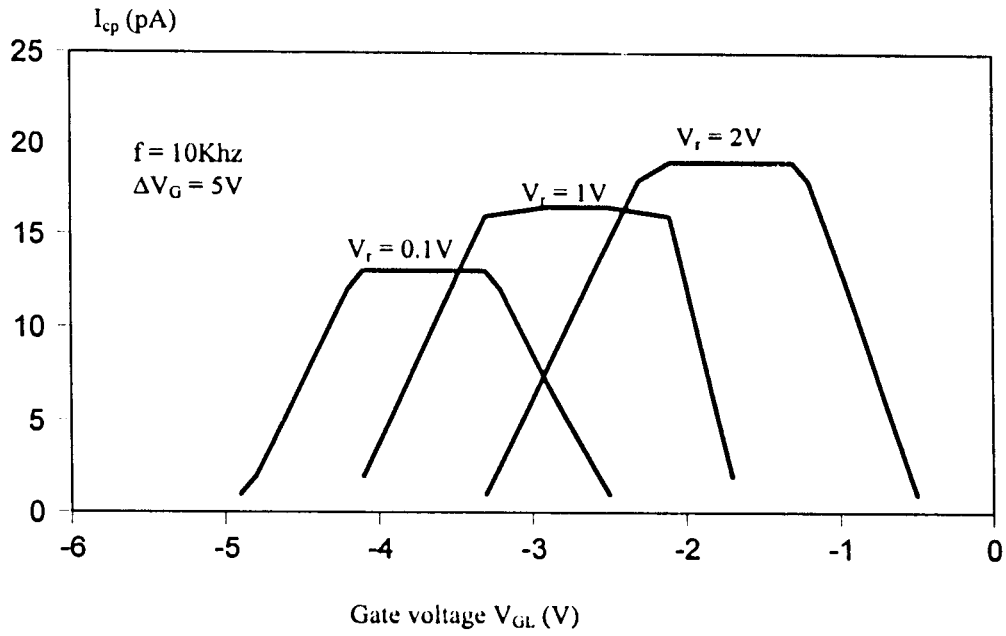

Fig.5.2 Elliot curves with different reverse bias voltages

5.3 Brugler's and Groeseneken's Curves

For the sake of comparaison with other data published by other authors[9,14,20], a set of charge pumping current curves have been obtained. Fig.5.3 shows the charge pumping current I_{cp} versus frequency for a high level gate voltage V_{GH} = 0V, source-drain reverse voltage V_r=0.1V and a pulse amplitude of 8V. We can see the linear dependence of the charge pumping current I_{cp} as a function of frequency within the range of

100Hz to 1Mhz (4 decades). We should note that only the upper curve has been reported in the litterature [9,10], which corresponds in our case to large values of the gate pulse width τ. However, the other curves corresponding to smaller values of gate pulse width τ (10nsec,20nsec) have not been reported yet in the published litterature.

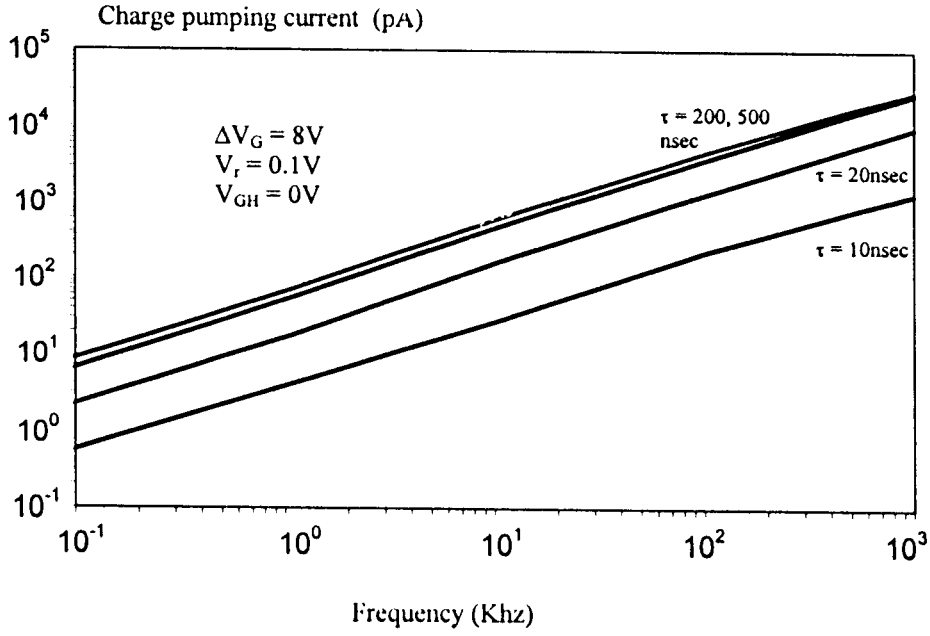

Fig.5.3 Charge pumping current versus frequency for different pulse widths

On the other hand, the curve given by [9] have been obtained using square pulses with a pulse width of 20μsec and a changing frequency up to 2Mhz. In the above reference, the charge pumping current has been modelled by the relationship $I_{cp} = fA_G q^2 \overline{D}_{it} \Delta\psi_s$, and no effect of pulse width has been reported. The interpretation for this, is that the curves reported in

references [9,14] corresponds to an equilibrium state. Which means that all the interface states have enough time to charge and discharge in response to the gate signal.
We have tried to focus more on this effect through the results we have shown in Fig.5.4 below,

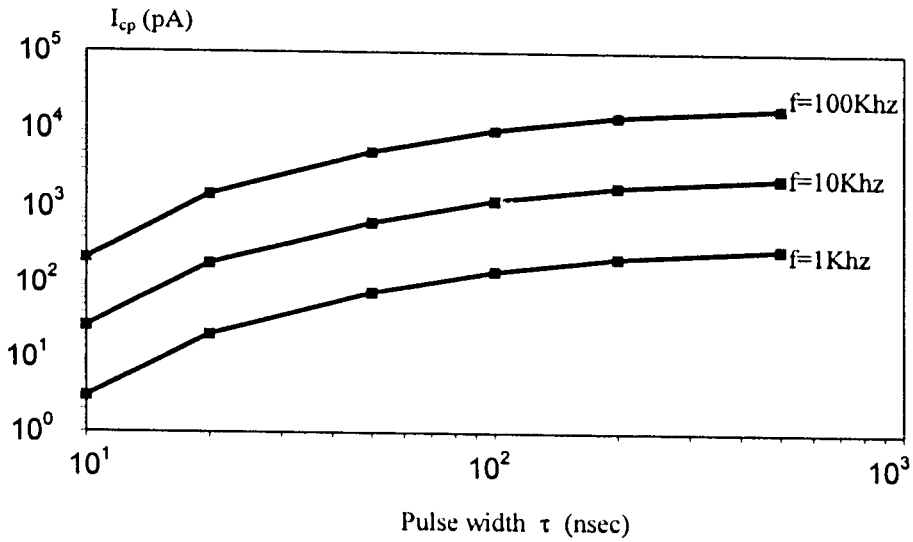

Fig.5.4 Charge pumping current versus pulse width for different frequencies

To have a better idea on the steady and the non-steady state behaviors, it is important to consider a one trap level model that has been elaborated by Simons and Wei [39,40]. As it is reported in these references, if the interface states can emit charges at the rate the gate charge changes, these states are in dynamic equilibrium with the conduction band, and hence,

$$\left|\frac{dQ_g}{dt}\right| = \left|\frac{dQ_t}{dt}\right| \qquad (5.1)$$

But, in non-equilibrium state, $\left|\frac{dQ_t}{dt}\right|$ is a function of the amount of charge in these states, and the above equation is no longer valid. Hence,

$$\left|\frac{dQ_g}{dt}\right| > \left|\frac{dQ_t}{dt}\right| \tag{5.2}$$

And so, the effective density of states seems to be less in case of non-steady state regime.

The results we have obtained and shown in Fig.5.4, show that the steady state regime, corresponding to saturation of the charge pumping current I_{cp} versus gate pulse width τ, is reached only for some higher values of gate pulse width τ. The equation

$$I_{cp} = fA_G q^2 \overline{D}_{it} \Delta\psi_s \tag{5.3}$$

is only valid for relatively larger values of pulse width τ.

This equation may be modified to be valid for any value of pulse width τ by replacing $\overline{D}_{it}$ by $\overline{D}_{it}^{\bullet}$, where $\overline{D}_{it}^{\bullet}$ is the effective density of states responding to a given gate voltage pulse.

Hence, the charge pumping current I_{cp} may be written as,

$$I_{cp} = fA_G q^2 \Delta\psi_s \overline{D}_{it}^{\bullet} \tag{5.4}$$

and the non-steady state trapped charge $Q_t(t)$ at any time t is given by Simmons and Wei [39,40] as,

$$Q_t(t) = qN_{st}kT\ln\left[1-\left(1-e^{(E_i-E_m(O))/kT}\right)\exp\left(-v\sigma N_c t e^{(E_i-E_s)/kT}\right)\right] \qquad (5.5)$$

In fact, the plot of the ratio (I_{cp}/f) versus the frequency f has been used by many authors [14,41] to determine the density of states. In our case it is clear that we get many intercepts of (I_{cp}/f) on f-axis, which means that we get many $\overline{D}_{it}$ values for the same device, in particular for small values of the pulse width τ. We can notice that for different higher values of pulse width τ the intercepts give approximately the same results, *i.e*, the same value of $\overline{D}_{it}$.

5.4 Charge Pumping Current Versus Gate Voltage Levels

In order to investigate the effect of the gate voltage, high and low levels, a set of experiments has been performed on our devices. The curves shown in Fig.5.5 have been obtained for a frequency of 1Khz, a reverse voltage V_r of 1V and a fixed V_{GL} of -8V. These curves, plotted in a logarithmic scale, show the variations of I_{cp} as a function of the high level gate voltage V_{GH} for a fixed V_{GL} . Note the strong dependence of I_{cp} on the pulse width τ.

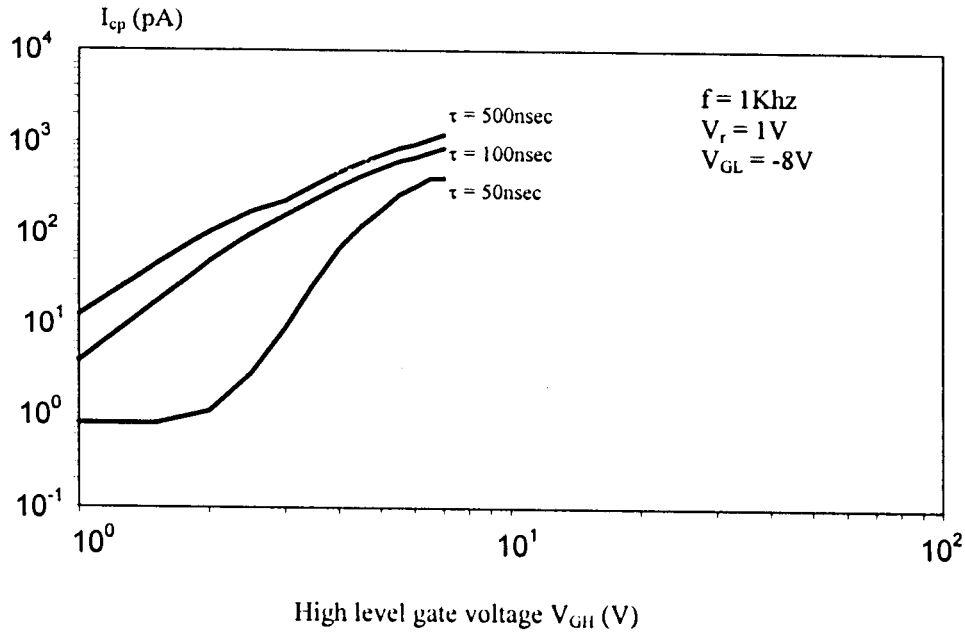

Fig.5.5 Charge pumping current versus high level gate voltage for different pulse widths.

For low values of V_{GH} (less than 3V) and for higher values (greater than 9V), eventhough there is some change in the charge pumping current I_{cp} for different values of the pulse width τ, it remains relatively smaller with respect to the change of the charge pumping current I_{cp} with the pulse width τ for intermediate values of V_{GH} ($3V < V_{GH} < 9V$). This effect can be explained by the fact that for smaller values of V_{GH}, the charge pumping current I_{cp} is small and no appreciable change can be observed for different values of pulse width τ. The same conclusion can be applied for higher values of V_{GH}, since the current is much higher and the device goes deeper in accumulation and depletion. However, for intermediate values of V_{GH} the appreciable change of the charge pumping current I_{cp} as a function of gate pulse width τ can be explained by the fact that the traps which are in a

non-steady state can not respond to short pulse widths. On the other hand, the medium change of V_{GH} is not enough to help the traps to respond to V_G as it is the case for higher values of V_{GH}.

These curves can be a very important starting point to study and explain the kinetics of interface states for the system SiO_2-Si and may be used for other Insulator-Semiconductor interfaces as well. Within the same idea, the charge pumping current has been measured as a function of the low level gate voltage V_{GL} for the same frequency as above (1Khz) , a reverse source-drain voltage V_r of 0.1V and a pulse amplitude ΔV_G of 5V. The results we have obtained are shown in Fig.5.6 below. Note again the dependence of the charge pumping current I_{cp} versus V_{GL} for different values of the gate pulse width τ.

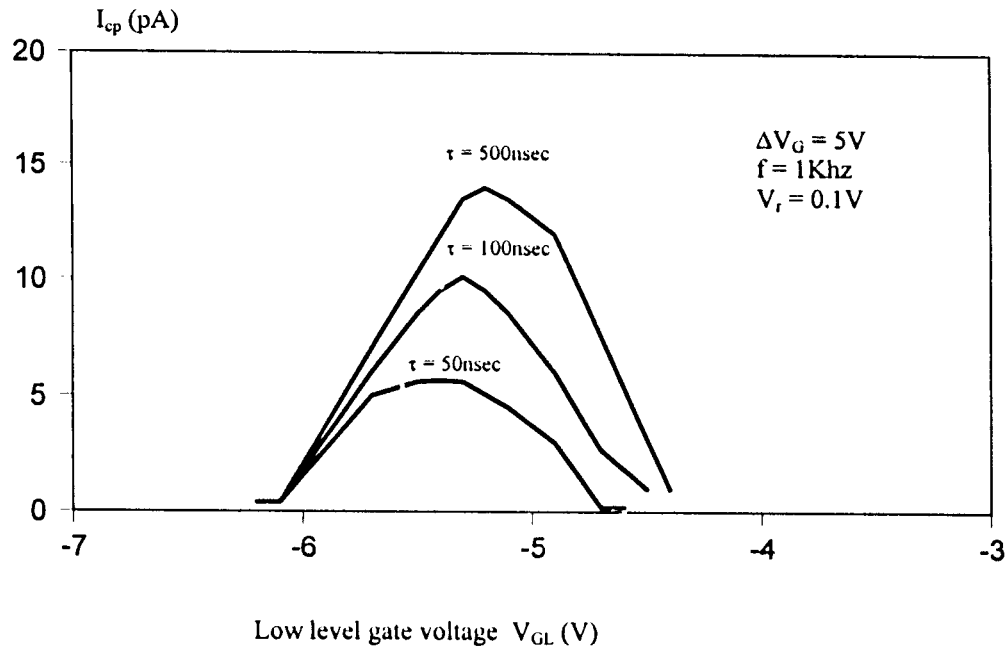

Fig.5.6 Charge pumping current versus low level gate voltage for different pulse widths

5.5 Effect of Pulse Width on the Charge Pumping Current

Another set of experiments has been carried out for the measurements of the charge pumping current I_{cp} versus the gate pulse width τ , for a certain number of different frequencies.

Typical results we have obtained are shown in Fig.5.7.

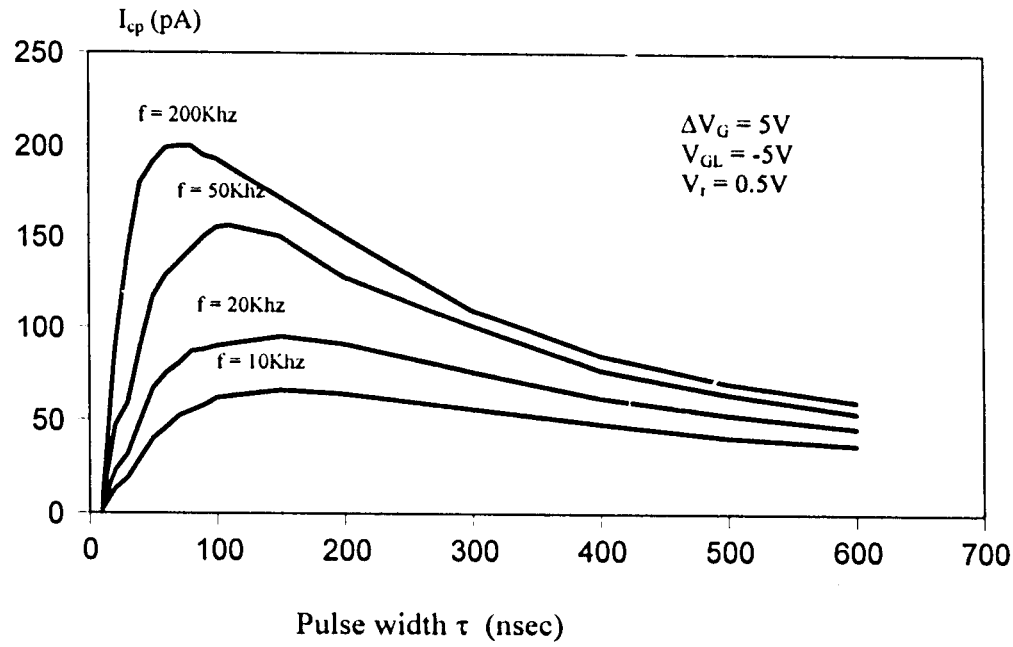

Fig.5.7 Charge pumping current versus pulse width for different frequencies

It is apparent from these curves that all the charge pumping curves show maxima for different values of the gate pulse width τ. These maxima increase in amplitude for increasing frequency. To our knowledge, these curves have not been reported before in the litterature which deals with the charge pumping technique.

The observed increase in the charge pumping current I_{cp} (left side of curves) for smaller values of pulse width τ can be explained by the fact that, firstly, the charge pumping current increases with frequency and secondly, when gate pulse width τ increases more states respond to the gate signal. The increasing process will reach a maximum level and then it goes down for higher values of the gate pulse width τ.

5.6 Effect of Frequency

Another set of data has been obtained for the charge pumping current as a function of a wide range of frequencies. Again, the curves of the charge pumping current versus frequency exhibit maxima for different values of the pulse width τ. We can see that the charge pumping current I_{cp} decreases more rapidely after saturation for higher values of gate pulse width τ. The maximum value of the current is obtained for a value of τ =50nsec.

Previous works [9,14] have reported the increase of the charge pumping current I_{cp} as a function of frequency for a fixed value of gate pulse width τ and they have expected the decrease of the charge pumping current I_{cp} for higher frequencies. But no results have been reported or expected the dependence of the charge pumping current I_{cp} on the gate pulse width τ.

The results we have obtained are shown in Fig.5.8, below,

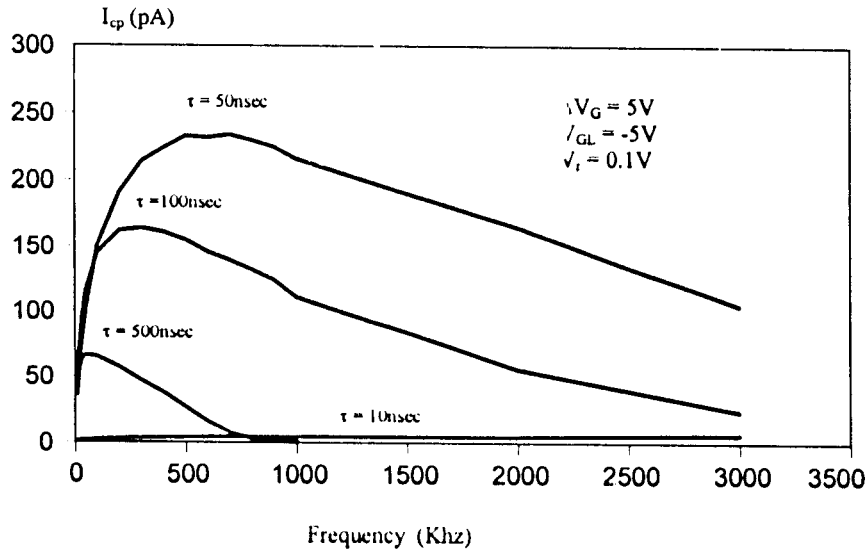

Fig.5.8 Charge pumping current versus frequency for different pulse widths (linear scale)

These results are plotted in a linear scale in Fig.5.8 and in a semilogarithmic scale in Fig.5.9 to make in evidence the changes of the charge pumping current I_{cp} for low values of frequency.

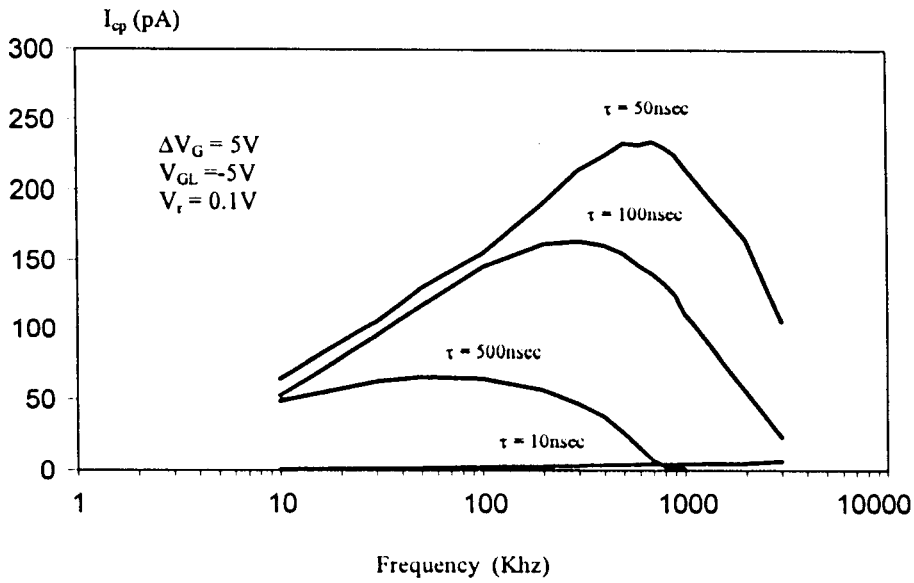

Fig.5.9 Charge pumping current versus frequency for different pulse widths (semilog scale)

These curves which have not been observed before and not reported in the litterature, show some maxima of the charge pumping current I_{cp} as a function of frequency for different values of gate pulse width τ. Also, the maximum value of the charge pumping current I_{cp} does not correspond neither to the higher value of the gate pulse width τ nor to the smallest value. But the maximum value of the charge pumping current I_{cp} corresponds to some intermediate value, in our case to a value of pulse width $\tau = 50nsec$ for a frequency of 700Khz.

This behavior has not been expected by any model in the litterature. However, the model proposed by Wachnik *et al* [18] which is an improved version of a previous model elaborated by Golder *et al* [12] and Backensto *et al* [13] can be considered as a good starting point to understand our results. In fact, this model for the charge pumping current is based on small rectangular voltage pulses and uses the Shockely-Read-Hall statistics for a single trap center. This model can be adapted to explain some of the results we have obtained, in particular those related to the existence of peaks of the charge pumping current I_{cp} versus the gate pulse width τ.

Before going into some details of the behaviors of our results, let's give the main ideas of the model given by Wachnik *et al* [18].

In fact, the model is based on the application of small square gate pulses to MOSFETs so that the surface remains pulsed around midgap between the flatband and the threshold voltages V_{FB} and V_T respectively.

And, since the charge pumping current is a result of recombination processes which consists of a capture of carriers from one band followed by capture of carriers from the other band, the authors have divided the capture sessions into two periods. During T_+ , in which the structure is weakly inverted, the states capture electrons from the conduction band and emit holes to the valence band, and during T_- , after the inversion layer disappears, holes are captured from the valence band by electron-filled states, and electrons are emitted by the conduction band (refer to Fig.3.4).
Using the SRH statistics, the return to equilibrium for traps is governed by the first order rate equation which is written as,

$$\frac{dn_t^-}{dt} = c_n n_t^0 - e_n n_t^- - c_p n_t^- + e_p n_t^0 \qquad (5.6)$$

Note that, since the traps at SiO_2-Si interface are distributed in energy it is evident that the calculation of the charge pumping current I_{cp} should be done over all the distribution section. The situation may be further simplified by specifying different discrete types of traps.

From the SRH statistics, the capture rates of electrons and holes c_n and c_p are related exponentially to the surface potential ψ_s , and that the electrons capture rate is much greater than holes capture rate during T_+ and it is much less than the hole capture rate during T_- . The region in which these two capture rates become approximately equal with an energy width less than kT is determined by σ_n/σ_p, which is the ratio of the capture cross sections.

To validate their model, they stated that only the states between E_{T-} and E_{T+} (where E_{T-} and E_{T+} are those traps near to the midgap defined as E_{T-} where $(e_n/c_n)=1$ and E_{T+} where $(e_p/c_p)=1)$), are the only states needed in calculating the charge pumping current I_{cp} (refer to Fig.3.5 and Fig.3.6).

Since they correspond to the set of traps which capture carriers during each period of the gate pulse cycle.

Between the energies E_{T+} and E_{T-} capture is the faster process by which traps change occupancy to return to equilibrium and above and below these energies emission dominates the return to equilibrium.

And from the dynamics of the capture process during the period T_+ and T_- they have derived an expression for the number of occupied traps at time t after the transition from the negative to the positive part of the pulse. The expression is given as follows, [18]

$$n^0{}_{T+}(t) = \frac{N_t\left(1-e^{-c_pT_-}\right)e^{-c_nt}}{1-e^{-\left(c_nT_+ + c_pT_-\right)}} \qquad (5.7)$$

And after the transition from the positive to the negative part of the pulse,

$$n^{-}_{T-}(t) = \frac{N_t\left(1-e^{-c_n T_+}\right)e^{-c_p t}}{1-e^{-\left(c_n T_+ + c_p T_-\right)}} \tag{5.8}$$

Where the charge pumping current I_{cp} can be calculated by considering the total number of holes captured during T_- , or from the total number of electrons captured during T_+ , in the energy range of sweep of V_G. That is, [18]

$$I_{cp} = qfA_G \int_{E_i}^{E} \int_{0}^{T} dt dE_T D_{it}\left(E_T\right) c_p f^{-}_{T-}\left(E_T, t\right) \tag{5.9}$$

Evaluating the time integral, one obtains, [18]

$$I_{cp} = qfA_G \int_{E_i}^{E} dE_T D_{it}\left(E_T\right) \frac{\left(1-e^{-c_p T_-}\right)\left(1-e^{-c_n T_+}\right)}{1-e^{-\left(c_n T_+ + c_p T_-\right)}} \tag{5.10}$$

It has been assumed in the above equations that the surface concentration of carriers is uniform.

The high frequency behavior proposed by the model goes to some saturation value of the charge pumping current I_{cp} independently of frequency. In other words, when T_+ and T_- become small compared to the inverse capture rates, and for a duty cycle of 50%, $T_+ = T_- = \frac{1}{2f}$, using Taylor's series it yields,

$$I_{cp} = \frac{qA_G}{2} \int_{E_i}^{E} dE_T D_{it}\left(E_T\right) \frac{c_p c_n}{c_p + c_n} \tag{5.11}$$

This conclusion does not agree with our experimental results, since there is neither saturation of the charge pumping current I_{cp} nor an independence of frequency at higher frequencies [27]. We can say that at higher frequencies (above some Mhz) many interface states will not respond to the gate signal, as it has been shown using C-V techniques at low temperature and high frequencies [5,27]. The explanation of the decrease of the charge pumping current I_{cp} at high frequencies is due mainly to the decrease of the number of states that respond to the gate pulses at these frequencies. Since the charge pumping current is a consequence of a recombination process, it certainly decreases when the effective number of recombination centers decreases. It is why the charge pumping current I_{cp} becomes practically zero at very high frequencies since the states will have no time neither to capture nor to emit free carriers from and toward the energy bands.

According to the authors [5,27], the saturation in the high frequency limit arises, first, from the cancellation of increase in pulse repetitions, and second, by the decrease in charge captured during each pulse, which do not agree of course with our results, neither from the numerical point of view nor from the experimental results.

In fact, from the experimental point of view, in the experiments they have carried out, the transition time of 25nsec has been used during all their work, which they consider of no effect on the charge pumping current I_{cp} . However, in our case, the pulse durations were less than their transition

times, and yet some variations have been noticed on the measured charge pumping current I_{cp} . In fact, we have tried to use equation (5.10) and we have written it as follows

$$I_{cp} = kf \frac{\left(1-e^{-c_p T_-}\right)\left(1-e^{-c_n T_+}\right)}{1-e^{-\left(c_n T_+ + c_p T_-\right)}} \tag{5.12}$$

Where k is the term $qA_G \int_{E_I}^{E} dE_T D_{it}(E_T)$ supposed independent of frequency f.

If we take the gate pulse width τ as being equal to T_+ and since $f = \frac{1}{\tau + T_-} = \frac{1}{T}$, where T is the period of the pulse, equation (5.12) can be written as a function of τ as,

$$I_{cp}(\tau) = k \frac{1}{T} \frac{\left(1-e^{-c_p(T-\tau)}\right)\left(1-e^{-c_n \tau}\right)}{1-e^{-\left(c_n \tau + c_p(T-\tau)\right)}} \tag{5.13}$$

Furthermore, if we compute the rate of change of the charge pumping current with respect to the pulse width $\frac{dI_{cp}(\tau)}{d\tau}$, we notice that it becomes equal to zero for some value of τ_m , and that this τ_m corresponds to a maximum of the charge pumping current I_{cp} . This maximum is, in addition, a function of frequency f. That is, this maximum shifts towards higher frequencies. Exactly as it is given by our experimental results. Hence, the derivative of (5.13) gives,

$$\frac{dI_{cp}(\tau)}{d\tau} = k\frac{1}{T}\frac{-c_p e^{-c_p(T-\tau)}\left(1-e^{-c_n\tau}\right)-e^{-c_p(T-\tau)}c_n e^{-c_n\tau}}{\left(1-e^{-c_n\tau+c_p(T-\tau)}\right)} + \frac{\left(1-e^{-c_p(T-\tau)}\right)\left(1-e^{-c_n\tau}\right)}{\left(1-e^{-c_n\tau+c_p(T-\tau)}\right)^2} * \left(-c_n-c_p\right)e^{-c_n\tau+c_p(T-\tau)} \quad (5.14)$$

Equation (5.14) can be solved numerically to determine τ_m . But, if we consider, for a first order approximation, the particular case where $c_n = c_p$, the value of τ_m which zeros equation (5.14) will be equal to $\frac{1}{2f}$. The simulated results for this case are shown in Fig.5.10 and Fig.5.11 below,

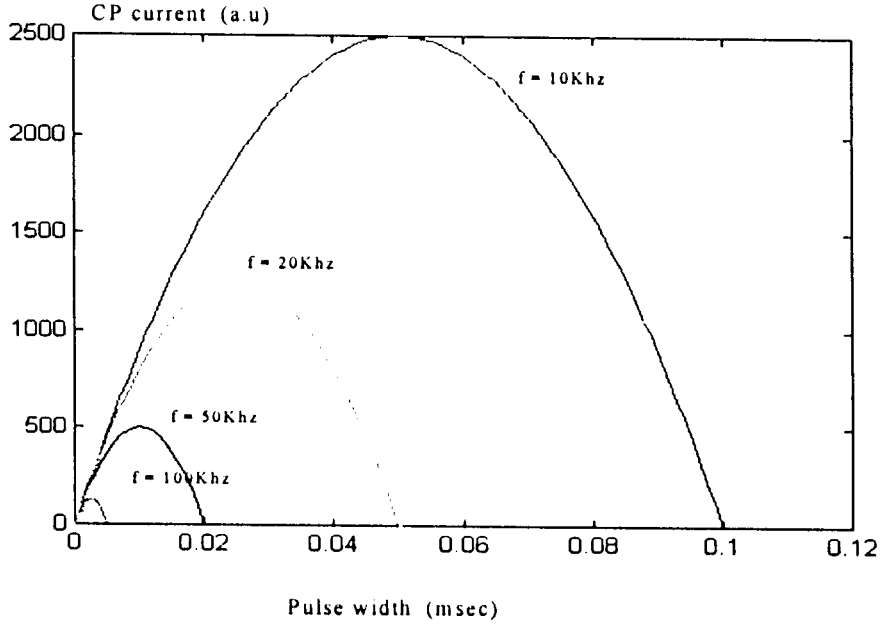

Fig.5.10 Charge pumping current versus pulse width for different frequencies

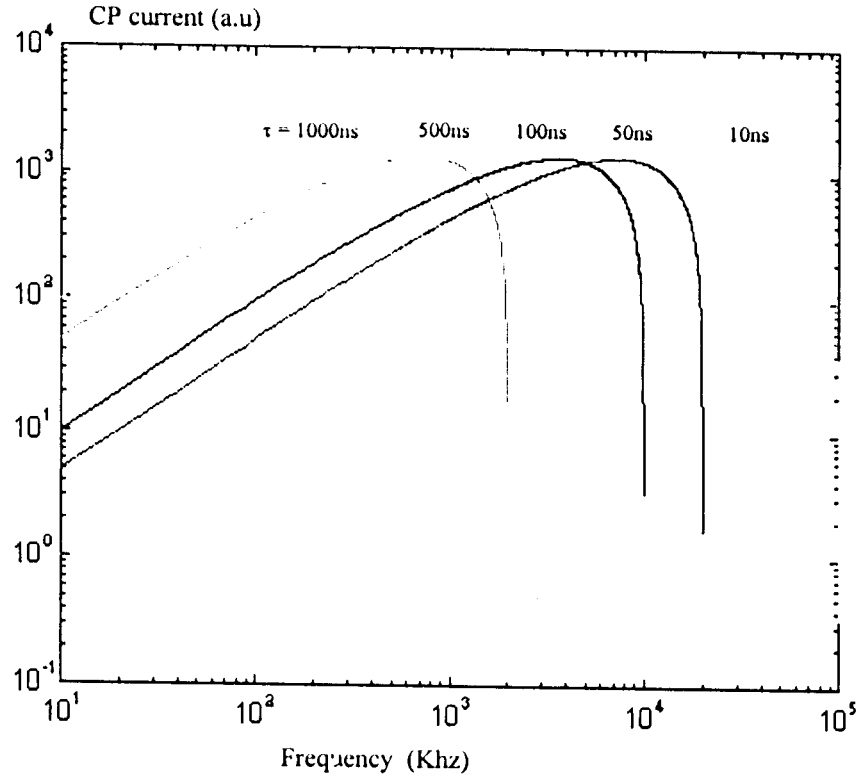

Fig.5.11 Charge pumping current versus frequency for different pulse widths

However, some deeper work related to modelling of the observed experimental behavior of the charge pumping current I_{cp} as a function of the pulse width τ should be done to determine the contribution of each parameter, such as σ_n , σ_p , c_n , c_p , D_{it} and so on. This will hopefully be a future work for another magister student.

We are convinced that a complete simulation will help to readjust the model proposed by Wachnik *et al* [18] and to explain some phenomenon not reported before. In particular, the profiles of σ_n , σ_p , and D_{it} , and their dependence on time.

5.7 Variation of Peak of I_{cp} with Frequency

We have also used the data we obtained for the charge pumping current I_{cp} , and tried to plot the family of peak values of the charge pumping current I_{cp} as a function of frequency for some given values of gate pulse width τ. One of the curves is shown in Fig.5.12 below. Note that the maximum peak value occurs at around 1Mhz for a value of pulse width τ = *50nsec*.

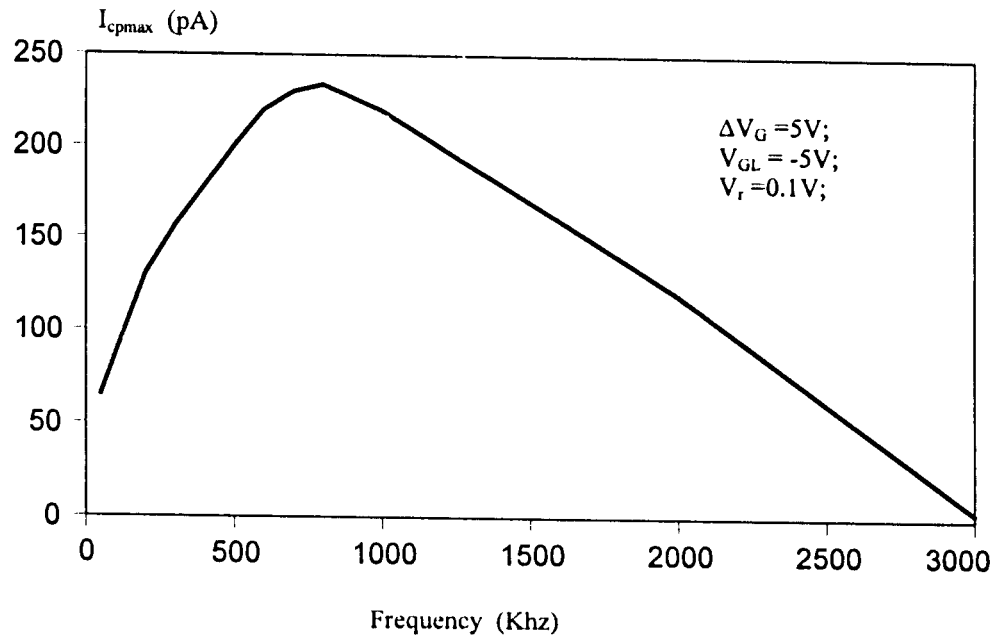

Fig.5.12 Peak values of the charge pumping current versus frequency

From this figure we can see the power of the charge pumping technique to characterize smaller integrated devices since we can always select the level of the charge pumping current I_{cp}

either through an appropriate choice of the pulse width τ or of the pulse frequency f.

Another curve of great importance is the one shown in Fig.5.13. This curve gives the profile of peaks of I_{cpmax} as a function of τ_m (corresponding to each maximum).

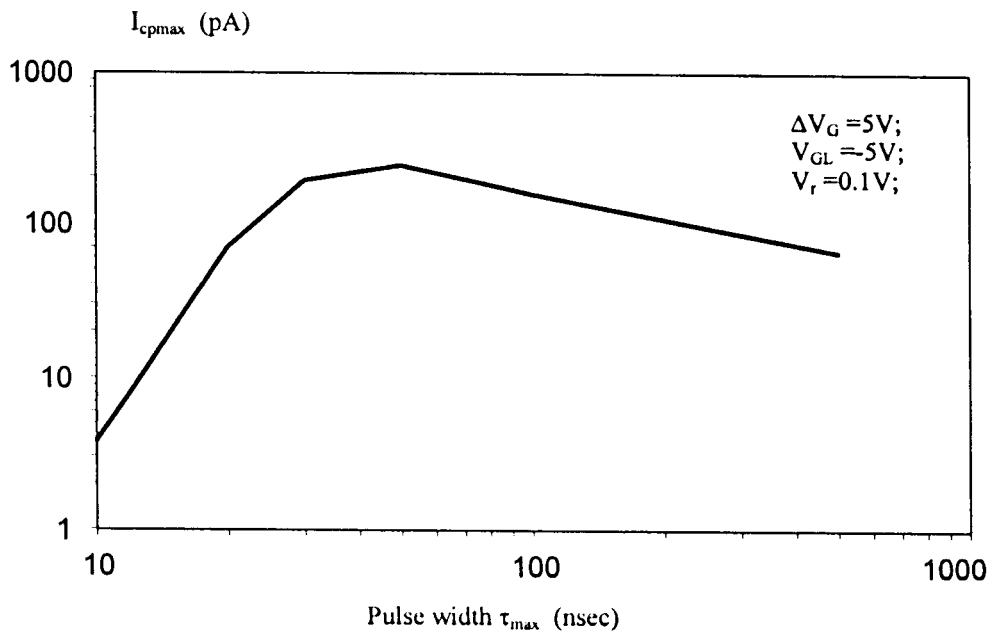

Fig.5.13 Peak values of the charge pumping current versus pulse width

Again we can notice that the maximum peak of the charge pumping current I_{cp} accurs around the value of the gate pulse width τ = *50nsec*. These values of the gate pulse width τ have not been considered in any of the experiments previously published.

At the end, we can conclude that very interesting and original results have been reported in this work, that may be used to build an improved charge pumping model that contributes to understand some of the parameters related to the interface of Oxide-Semiconductor devices. A complete simulation is needed to consider the various cases and values for the set of parameters that characterize the interface.

Chapter 6

CONCLUSION

In this work, we have investigated the charge pumping current of MOSFETs and its dependence on the time and voltage parameters of the input gate pulses. In fact, most of the published works are based on square and / or triangular gate voltages for MOS structures or MOS transistors. The proposed technique has been applied for submicron integrated MOSFETs and many non previously published results have been obtained which were presented in the previous chapter. Eventhough no new model has been proposed to explain the behavior of the charge pumping current on the change of the gate pulse parameters, in particular the pulse width, the model proposed by Wachnik *et al* can be slightly modified to describe the general behavior of our results.

Thanks to the device characterization system, we have been able to carry out an exhaustive experimental study of the charge pumping current variation with respect to different gate pulse parameters. So, the principal results obtained are :

1. The variation of the charge pumping current with respect to a new parameter which is the gate pulse width.
2. The dependence of the charge pumping current on the gate pulse levels for different gate pulse widths.
3. The existence of one maximum value of the charge pumping current variation with respect to the gate pulse width.
4. The maximum shifts towards lower values of gate pulse width with the increasing frequency.
5. The charge pumping current versus frequency exhibit maxima for different values of the gate pulse width.

We have proposed a new version of the charge pumping technique based on a variable gate pulse width. Some of the results obtained agree with those published by other authors which validate our data. Other results have been verified through simulation because, to our knowledge, no one has used the gate pulse width parameter to study the charge pumping current and hence the interface states.

From these considerations, we can say that this work can be a starting point to study and explain the kinetics of the interface states for the $Si-SiO_2$ system and may be used for other Insulator-Semiconductor interfaces as well. As a further step, we propose the elaboration of a more general model of the charge pumping current that will include the gate pulse width parameter. This could be achieved through more experimental work on a large set of testing devices and also a complete

simulation is needed to consider the various cases and values for the set of parameters that characterize the interface. We are convinced that it will help in understanding the different phenomena of emissions and captures by the interface states in the majority of the silicon bandgap especially in submicron transistors. And thus accurate simulators could be developed for the state of the art MOS VLSI circuits.

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