During the last three decades, digital relays have been widely used in power grid due to their flexibility and enhanced security and dependability properties. The decision of the digital protective device highly depends on the digital signal filtering computing the fundamental phasors of line voltages and currents. Several digital algorithms have been proposed in the literature for estimating the fundamental phasors, however, during a transient condition, line current and voltage may include unwanted components such as dc exponentially decaying associated with the harmonics and sub-harmonics. These digital algorithms always need few cycles for obtaining the accurate fundamental phasors which are undesirable in the protection field.The approach proposed in this work for reliable phasor estimation algorithm is first to remove disturbance signals using designed digital filter, then use conventional HCDFT or FCDFT algorithm to compute phasors with required accuracy and convergence speed. Besides, the combined optimized digital filter (ODF) and DFT algorithm are therefore used to quickly and accurately calculate the phasors. The obtained phasor algorithm has the required characteristics to remove the dc component and dump the sub-harmonic as well as harmonic components. The performance of the obtained phasor measurement algorithm is tested using estimated disturbance test signals and data obtained from series-compensated power system network simulation. Simulation results corroborate performance improvement of the proposed phasor estimation algorithm as compared with those obtained using classical cosine and Fourier phasor algorithms